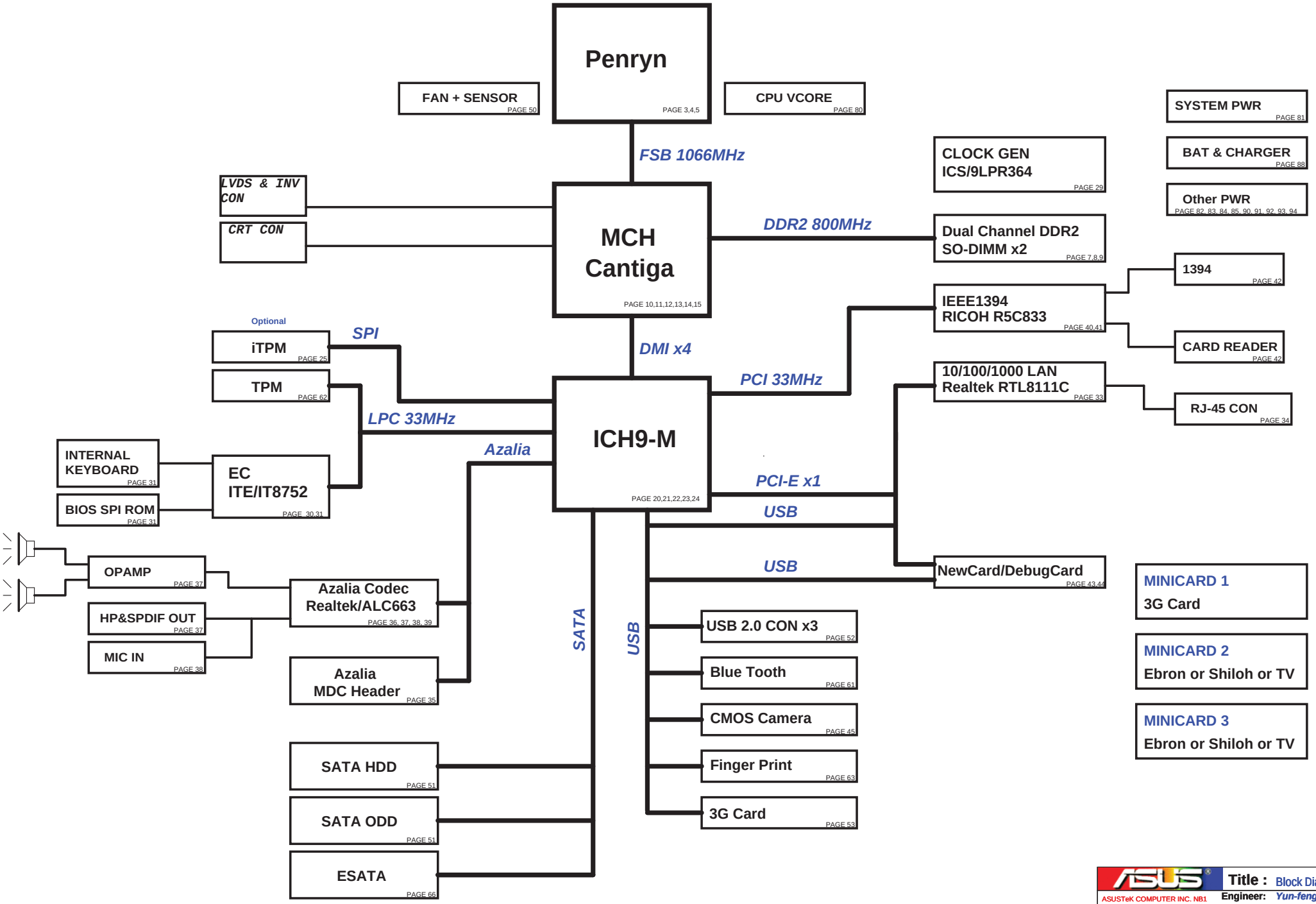
# N50A/N51A Montevina Block Diagram






| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : Block Diagram | |
| | Engineer: Yun-feng_yan | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Thursday, July 24, 2008 | Sheet 1 of 79 | |

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| 92 | POWER_PROTECT |
| 93 | POWER_SIGNAL |
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GPIO33 Internal Pull High, Go Low= Flash
Descriptor Security will be overriden

| ICH9-M GPIO | Use As | Signal Name | Power |
|---|---|---|---|
| GPIO 00 | GPI | PMSYNC#(programmed as GPO) | +3VS |
| GPIO 01 | GPI | DOCKING_DET# EXT PU | +3VS |
| GPIO [2:5] | GPI | PCI_INT[E:H]# EXT PU | +5VS |
| GPIO 06 | GPI | - EXT PU | +3VS |
| GPIO 07 | GPI | - EXT PU | +3VS |
| GPIO 08 | GPI | EXT_SMI# EXT PU | +3VSUS |
| GPIO 09 | Native | WOL_EN | +3VSUS |
| GPIO 10 | GPI | RTLAN_DSM# EXT PU | +3VSUS |
| GPIO 11 | Native | EXT_SCI#(Programmed as GPI | +3VSUS |
| GPIO 12 | GPO | - | +3VSUS |
| GPIO 13 | GPI | CB_SD#(Programmed as GPO) | +3VSUS |
| GPIO 14 | GPI | AC_PRESENT EXT PD | +3VSUS |
| GPIO 15 | Native | STP_PCI# | +3VSUS |
| GPIO 16 | Native | PM_DPRSLPVR INT PD* | +3VS |
| GPIO 17 | GPI | WLAN_LED(Programmed as GPO | +3VS |
| GPIO 18 | GPO | - | +3VS |
| GPIO 19 | GPI | - EXT PU | +3VS |
| GPIO 20 | GPO | - INT PD* | +3VS |
| GPIO 21 | GPI | - EXT PU | +3VS |
| GPIO 22 | GPI | BT_DET# EXT PU | +3VS |
| GPIO 23 | Native | ICH_LDRQ1# INT PU | +3VS |
| GPIO 24 | GPO | WLAN_ON | +3VSUS |
| GPIO 25 | Native | STP_CPU# | +3VSUS |
| GPIO 26 | Native | PM_S4_STATE# | +3VSUS |
| GPIO 27 | GPO | BT_ON | +3VSUS |
| GPIO 28 | GPO | BT_LED | +3VSUS |
| GPIO 29 | Native | NEWCARD_OC# | +3VSUS |
| GPIO 30 | Native | USB_OC3467# | +3VSUS |
| GPIO 31 | Native | USB_OC3467# | +3VSUS |
| GPIO 32 | GPO | PM_CLKRUN# | +3VS |
| GPIO 33 | GPO | - INT PU* | +3VS |
| GPIO 34 | GPO | - | +3VS |
| GPIO 35 | GPO | - | +3VS |
| GPIO 36 | GPI | - EXT PU | +3VS |
| GPIO 37 | GPI | PCB_ID0 | +3VS |
| GPIO 38 | GPI | PCB_ID1 | +3VS |
| GPIO 39 | GPI | PCB_ID2 | +3VS |
| GPIO 40 | Native | USB_OC01# | +3VSUS |
| GPIO 41 | Native | USB_OC2# | +3VSUS |
| GPIO 42 | Native | USB_OC3467# | +3VSUS |
| GPIO 43 | Native | USB_OC3467# | +3VSUS |
| GPIO 44 | Native | CLK_DEC# | +3VSUS |
| GPIO 45 | Native | CLK_ACC | +3VSUS |
| GPIO 46 | Native | WLAN_ON | +3VSUS |
| GPIO 47 | Native | UNDOCKING# | +3VSUS |
| GPIO 48 | GPI | EMAIL_LED# EXT PU | +3VS |
| GPIO 49 | GPO | GPU_RST# INT PU* | **+3VS** |
| GPIO 50 | Native | PCI_REQ#1 | +5VS |
| GPIO 51 | Native | PCI_GNT#1 INT PU* | +3VS |
| GPIO 52 | Native | PCI_REQ#2 | +5VS |
| GPIO 53 | Native | PCI_GNT#2 INT PU* | +3VS |
| GPIO 54 | Native | PCI_REQ#3 | +5VS |
| GPIO 55 | Native | PCI_GNT#3 INT PU* | +3VS |
| GPIO 56 | GPI | - EXT PU | +3VSUS |
| GPIO 57 | GPI | - EXT PU | +3VSUS |
| GPIO 58 | GPI | SPI_CS#1 INT PU* | +3VSUS |
| GPIO 59 | Native | USB_OC0# | +3VSUS |
| GPIO 60 | Native | RTLAN_DSM_EN | +3VSUS |

| EC GPIO | Use As | Signal Name | Power |
|---|---|---|---|
| GPA0 | GPO | PWR_LED_UP# | |
| GPA1 | GPO | CHG_LED_UP# | |
| GPA2 | GPO | BATSEL_3S# | |
| GPA3 | - | - | |
| GPA4 | GPO | LCD_BL_PWM | |
| GPA5 | GPO | FAN0_PWM | |
| GPA6 | GPO | BAT1_CNT1# | |
| GPA7 | GPO | BAT2_CNT1# | |
| GPB0 | GPO | CHG_EN# | |
| GPB1 | GPO | PRECHG | |
| GPB2 | GPI | DISTP# | |
| GPB3 | ALT | SMB0_CLK | |
| GPB4 | ALT | SMB0_DAT | |
| GPB5 | OD | A20GATE | |
| GPB6 | OD | RCIN# | |
| GPB7 | GPO | PM_RSMRST# | |
| GPC0 | GPI | MARATHON# | |
| GPC1 | ALT | SMB1_CLK | |
| GPC2 | ALT | SMB1_DAT | |
| GPC3 | GPO | PM_PWRBTN# | |
| GPC4 | ALT | AC_IN_OC# | |
| GPC5 | GPO | OP_SD# | |
| GPC6 | ALT | BAT1_IN_OC# | |
| GPC7 | GPO | 3G_ON# | |
| GPD0 | GPI | PWRLIMIT# | |
| GPD1 | ALT | PM_S4_STATE# | |
| GPD2 | ALT | BUF_PLT_RST# | |
| GPD3 | OD | EXT_SCI# | |
| GPD4 | OD | EXT_SMI# | |
| GPD5 | GPO | LCD_BACKOFF# | |
| GPD6 | ALT | FAN0_TACH | |
| GPD7 | GPI | COLOREN# | |
| GPE0 | GPO | VSUS_ON | |
| GPE1 | GPO | SUSC_EC# | |
| GPE2 | GPO | SUSB_EC1# | |
| GPE3 | GPO | CPU_VRON | |
| GPE4 | ALT | PWR_SW# | |
| GPE5 | ALT | BAT2_IN_OC# | |
| GPE6 | GPI | LID_SW# | |
| GPE7 | GPO | PM_THERM# | |
| GPF0 | GPI | BLUETOOTH# | |
| GPF1 | GPI | WIRELESS# | |
| GPF2 | ALT | PS2_CLK_5S_PD | |
| GPF3 | ALT | PS2_DATA_5S_PD | |
| GPF4 | ALT | TP_CLK | |
| GPF5 | ALT | TP_DAT | |
| GPF6 | GPO | THRO_CPU | |
| GPF7 | GPO | PS_SHDN# | |
| GPG0 | GPI | INSTANT_ON# | |
| GPG1 | ALT | PM_SUSB# | |
| GPG2 | GPO | BAT1_CNT2# | |
| - | - | - | |
| - | - | - | |

| EC GPIO | Use As | Signal Name | Power |
|---|---|---|---|
| - | - | - | |
| GPG6 | GPO | BAT2_CNT2# | |
| - | - | - | |
| GPH0 | OD | PM_CLKRUN# | |
| GPH1 | ALT | - | |
| GPH2 | ALT | - | |
| GPH3 | GPO | BAT_LEARN | |
| GPH4 | GPO | - | |
| GPH5 | GPO | NUM_LED | |
| GPH6 | GPO | CAP_LED | |
| - | - | - | |
| GPI0 | GPI | - | |
| GPI1 | GPI | SUS_PWRGD | |
| GPI2 | GPI | ALL_SYSTEM_PWRGD | |
| GPI3 | GPI | VRM_PWRGD | |
| GPI4 | GPI | PWR_MON | |
| GPI5 | GPI | PD_DET# | |
| GPI6 | GPI | KB_ID0 | |
| GPI7 | GPI | KB_ID1 | |
| GPJ0 | GPO | EC_CLK_EN | |
| GPJ1 | GPO | PM_PWROK | |
| GPJ2 | GPI | UNDOCK#_PD | |
| GPJ3 | - | - | |
| GPJ4 | GPO | BL_DA | |
| GPJ5 | GPO | FAN_DA | |
| GPK0 | GPI | PM_SLP_M# | |
| GPK1 | GPI | SUSPWR_ACK | |
| GPK2 | GPI | PM_SUSC# | |
| GPK3 | GPI | +3VM_PG | |
| GPK4 | GPI | +1.05VM_+3VMCLK_PG | |
| GPK5 | GPI | LAN_WOL_EN | |
| GPL0 | GPI | AC_APR_UC# | |
| GPL1 | GPI | - | |
| GPL2 | GPO | - | |
| GPL3 | GPO | LAN_RST# | |
| GPL4 | GPO | CL_PWROK | |
| GPL5 | GPO | EC_WLAN_PWR | |
| GPL6 | GPO | SLP_M_ON | |
| GPL7 | GPO | S4_STATE_ON | |
| GPK6 | GPO | AC_PRESENT | |
| GPK7 | GPI | PS_CPPE# | |

INT PU*: PU or PD in special time



ASUSTeK COMPUTER INC. NB1 Engineer: <OrgAddr1>

Title : Schematic Information

Size: Custom | Project Name: N50A/N51A | Rev: 1.0

Date: Thursday, July 24, 2008 | Sheet 2 of 79

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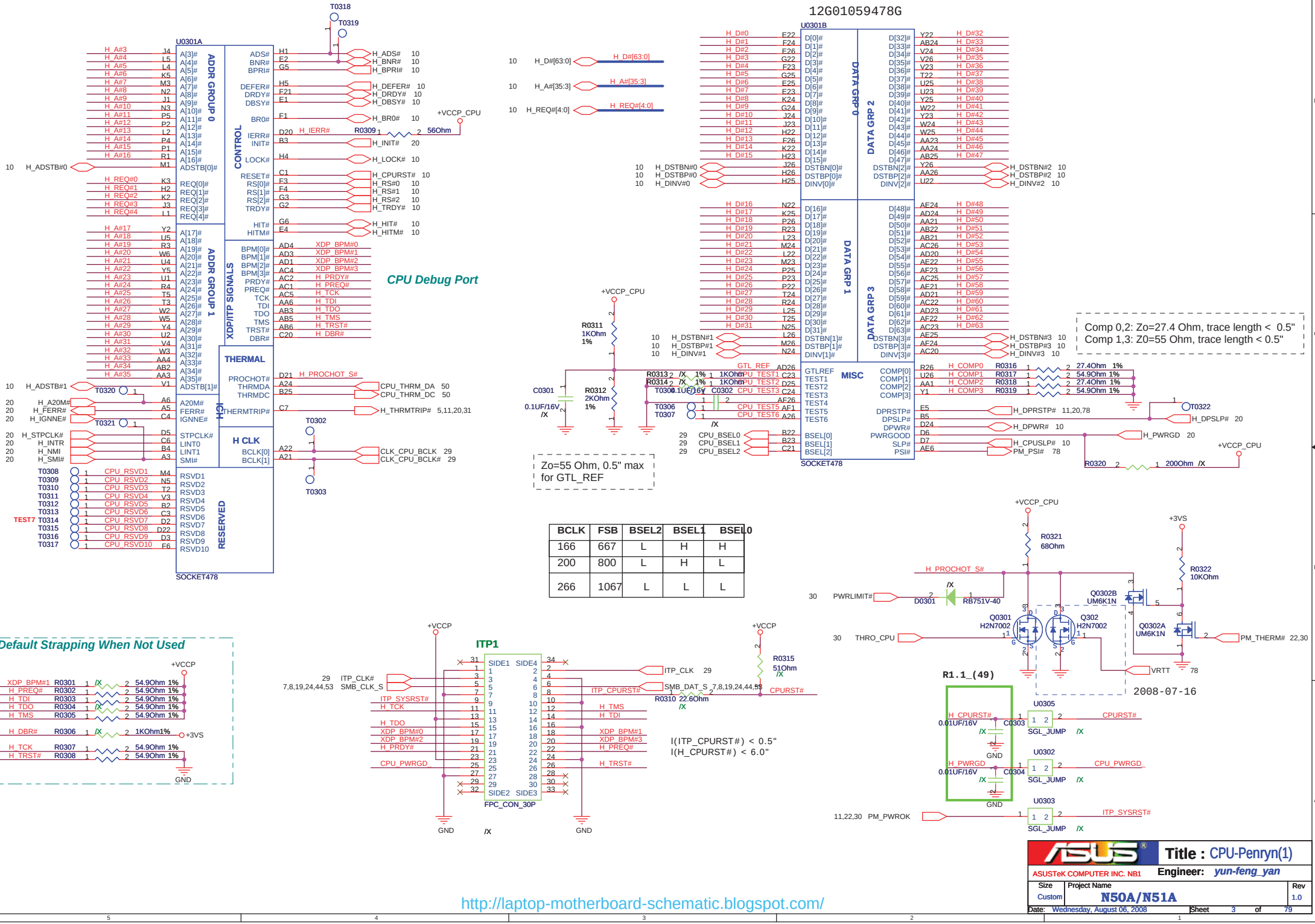



| BCLK | FSB | BSEL2 | BSEL1 | BSEL0 |
|---|---|---|---|---|
| 166 | 667 | L | H | H |
| 200 | 800 | L | H | L |
| 266 | 1067 | L | L | L |



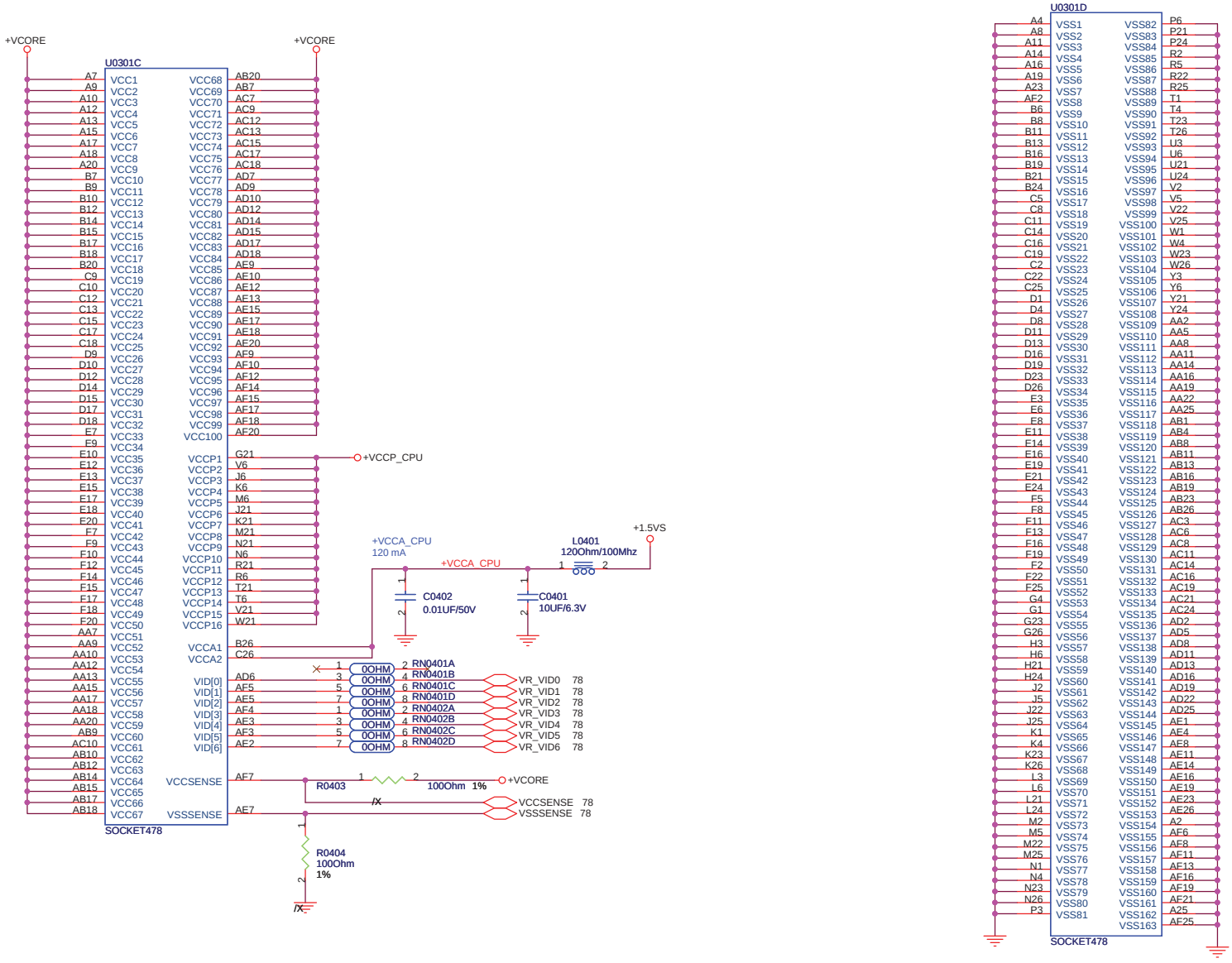
ASUSTeK COMPUTER INC. NB1

Title : CPU-Penryn(1)

Engineer: yun-feng_yan

| Size | Project Name | Rev |
|---|---|---|
| Custom | N50A/N51A | 1.0 |

Date: Wednesday, August 06, 2008 Sheet 3 of 79



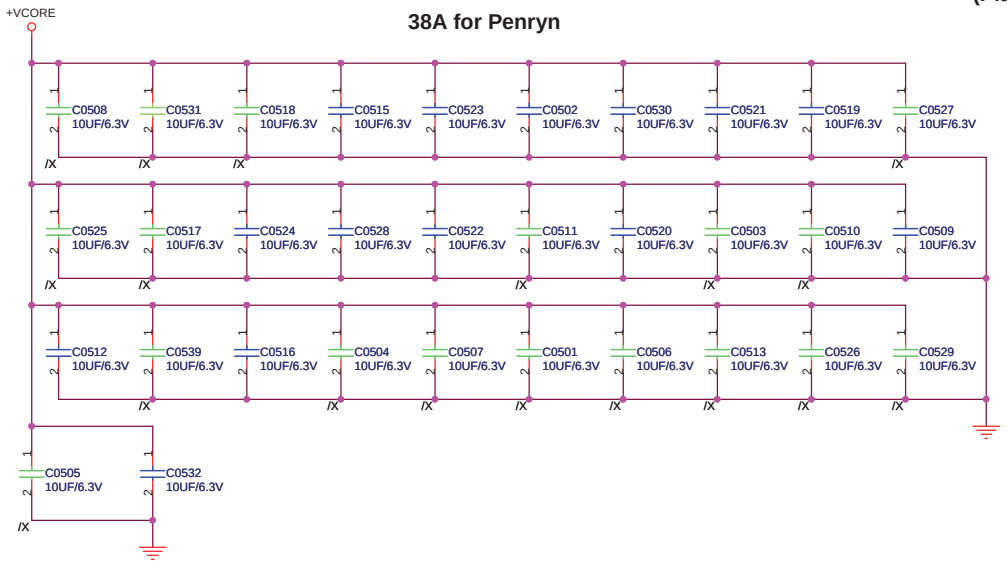






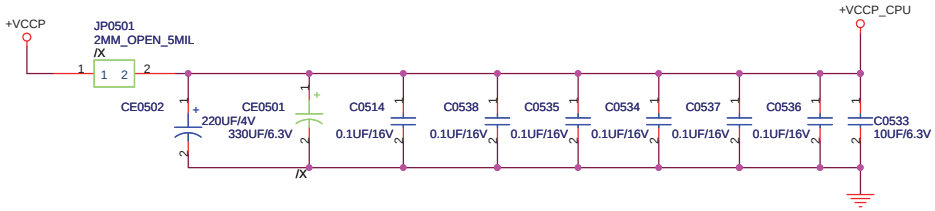
| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : CPU-Penryn(2) | |
| | Engineer: yun-feng_yan | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Friday, August 01, 2008 | Sheet 4 of 79 | |

## 38A for Penryn




## +VCCP Decoupling Capacitor (Place near CPU)

因爲CE0501與ME干涉,CE0501要移遠一點,而預留CE0502在原本CE0501位置

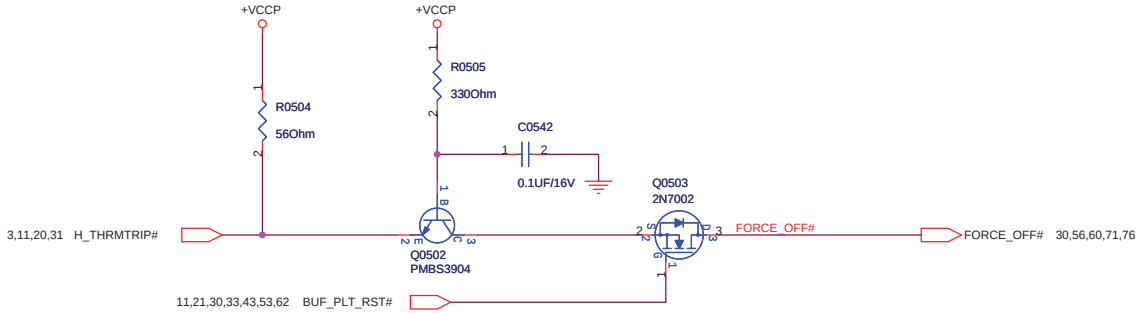



### Decoupling guide from Intel

| | | |
|---|---|---|
| VCORE | 22uF/10V r 10uF | * 32pcs |
| | 330uF/2V | * 6pcs |
| VCCP | 0.1uF | * 6pcs |
| | 150uF | * 1pcs ? |
| | 10uF | * 1pcs ? |

*+VCORE Mid-Frequency Capacitor*
*Intel: 22UF *32*
*F3S: 10UF *16*
*A7S: 10UF *10 ....11/17*
*V1V: ?*

*+VCCP Decoupling Capacitor*
*Intel: 270UF *1, 0.1UF *6*
*F3S: 100UF *1, 0.1UF *4*
*V1V: ?*




**Thermal Trip signal (From CPU to ICH-9M and sequence)**

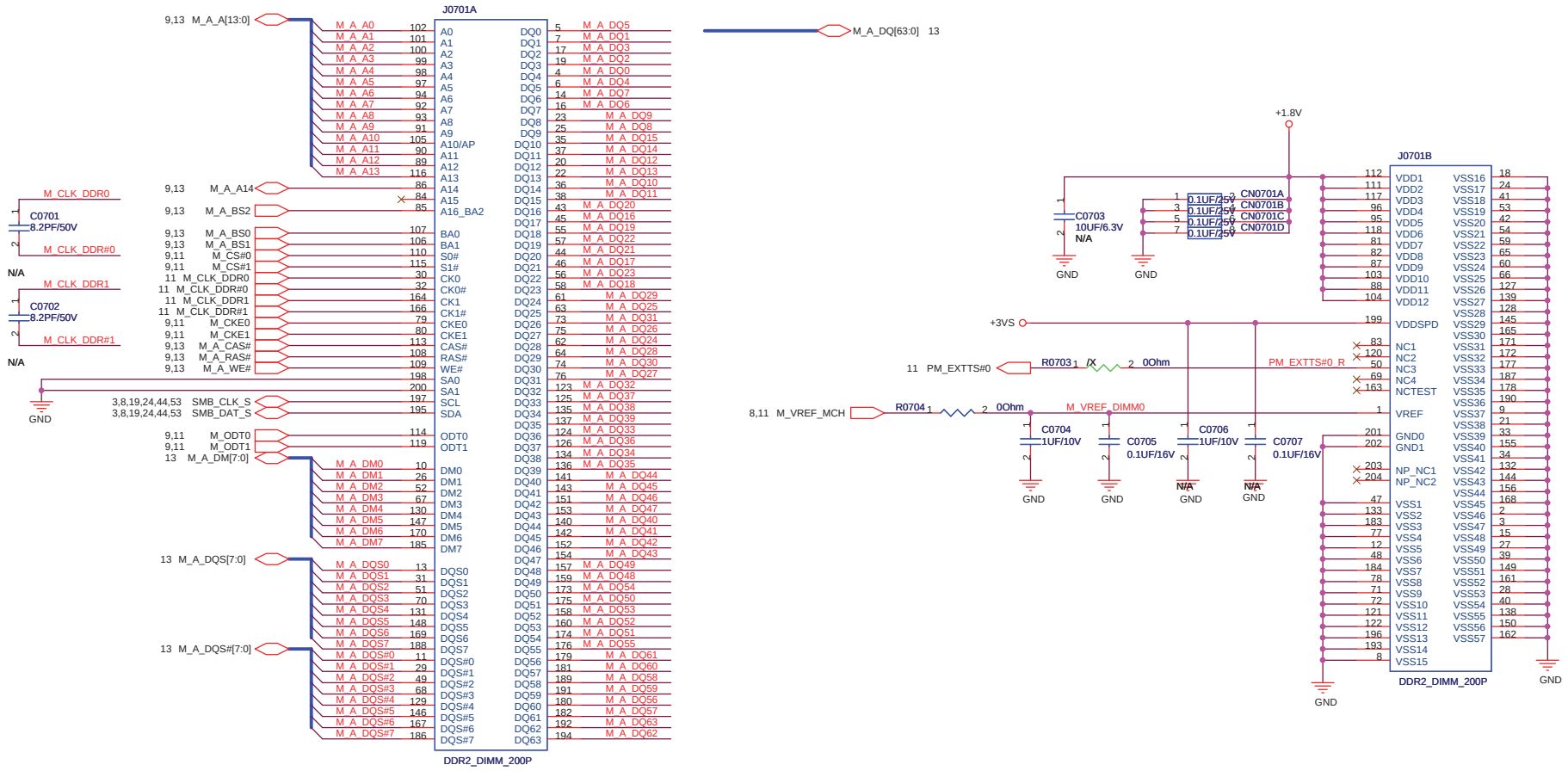
Thermal trip control circit



| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : CPU CAPS | |
| | Engineer: yun-feng_yan | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Friday, August 01, 2008 | Sheet 5 of 79 | |

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : | |
| | Engineer: yun-feng_yan | |
| Size: A | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Thursday, July 24, 2008 | Sheet 6 of 79 | |

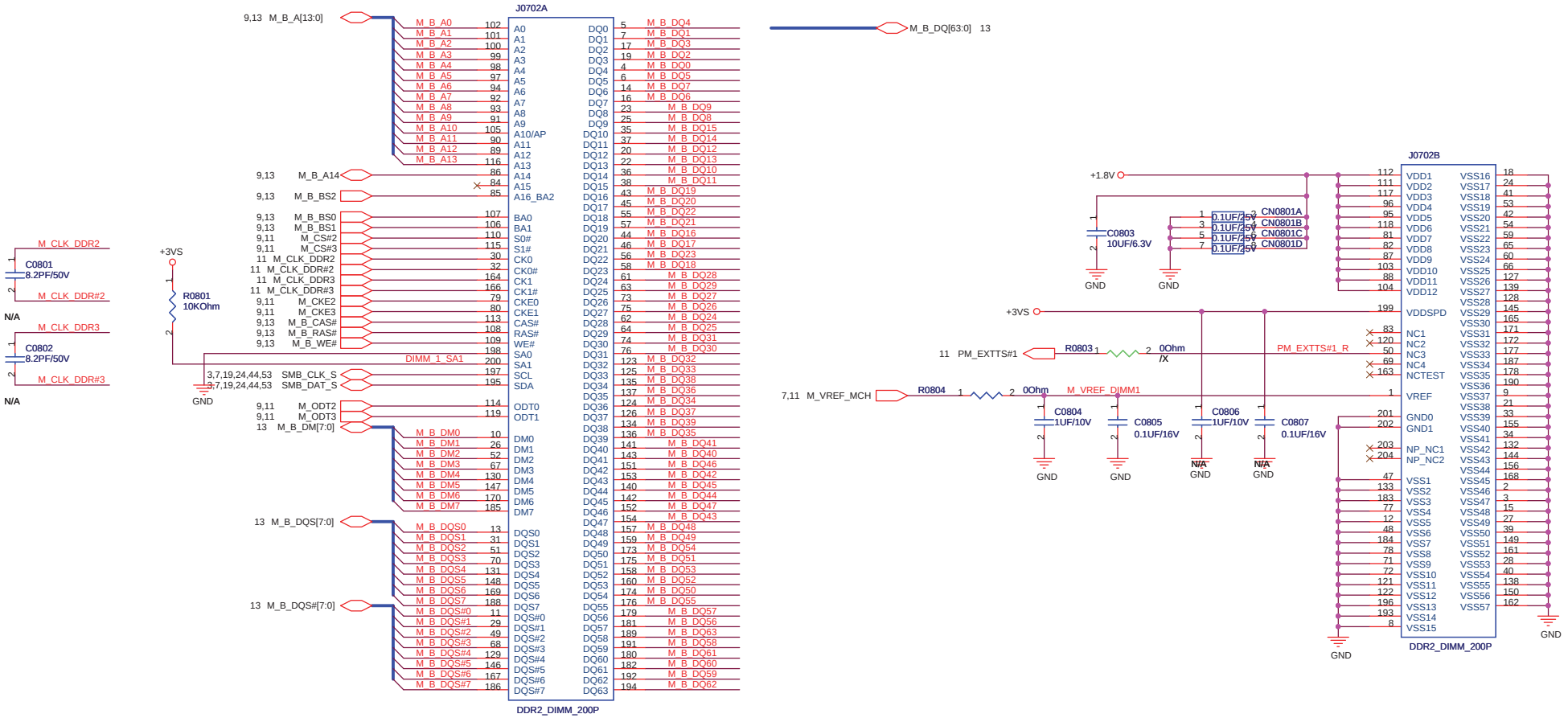
## REV Type





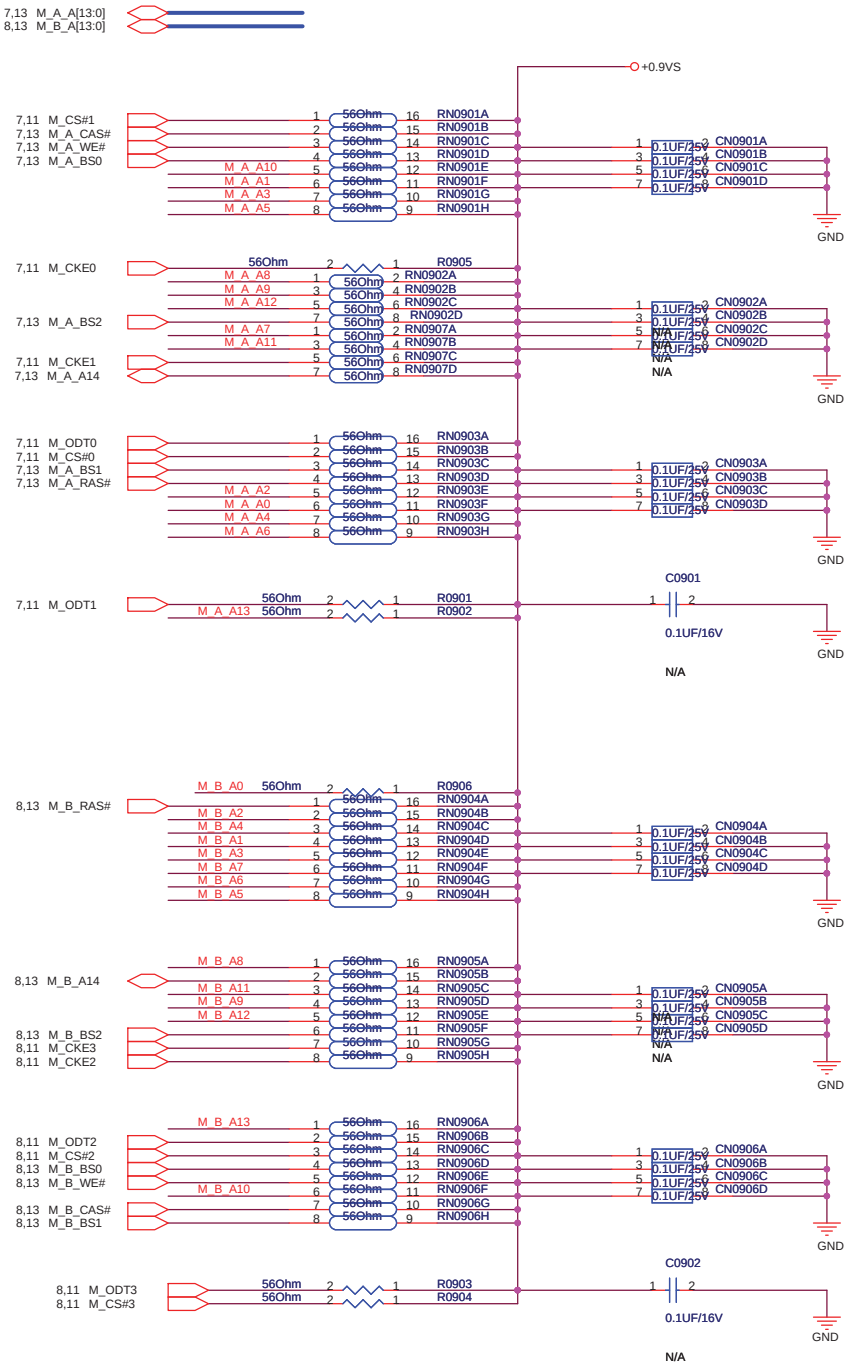

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title: DDR2 SO-DIMM_0 | |
| | Engineer: yun-feng_yan | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 7 of 79 | |

## STD Type



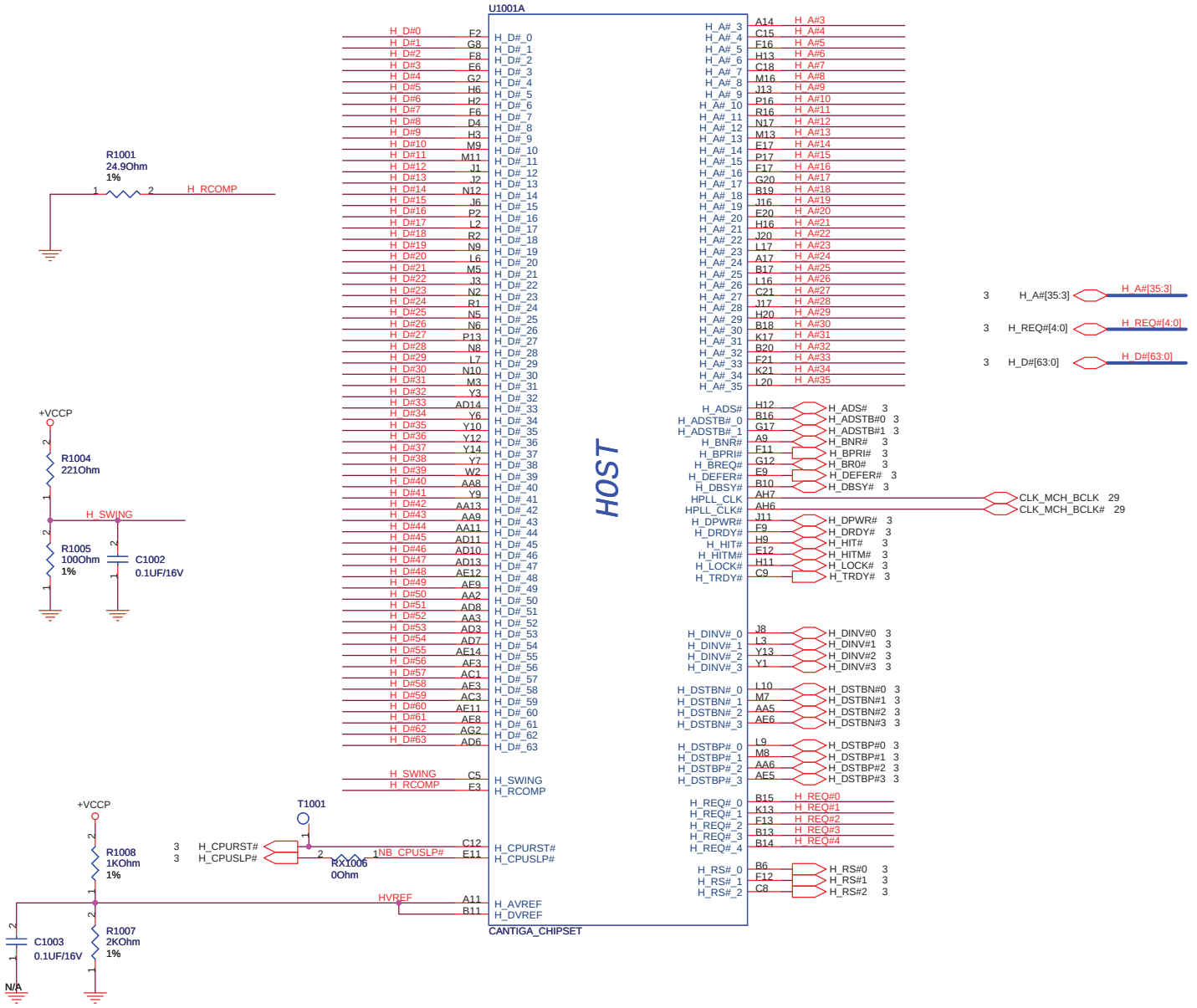

| | | | |
|---|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Engineer: yun-feng_yan | | |
| Size: Custom | Project Name: N50A/N51A | | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 8 of 79 | | |

Title :DDR2 SO-DIMM_1






| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title DDR2 termination | |
| | Engineer: yun-feng_yan | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 9 of 79 | |




Cap 0.1uF within 100 mils from GMCH



| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : Cantiga -- CPU (1) | |
| | Engineer: yun-feng_yan | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 10 of 79 | |

U1001B

## ME JTAG PORT

T1122 ME_JTAG_TCK
T1123 ME_JTAG_TDI
T1124 ME_JTAG_TDO
T1125 ME_JTAG_TMS
T1126

R1130 0Ohm /X

RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 RSVD7 RSVD8 RSVD9 RSVD10 RSVD11 RSVD12 RSVD13 RSVD14 RSVD15 RSVD16 RSVD17 RSVD20 RSVD21 RSVD22 RSVD23 RSVD24 RSVD25

RSVD

## DDR CONTROL/COMPENSATION

SA_CK_0 SA_CK_1 SB_CK_0 SB_CK_1 → M_CLK_DDR0 7, M_CLK_DDR1 7, M_CLK_DDR2 8, M_CLK_DDR3 8

SA_CK#_0 SA_CK#_1 SB_CK#_0 SB_CK#_1 → M_CLK_DDR#0 7, M_CLK_DDR#1 7, M_CLK_DDR#2 8, M_CLK_DDR#3 8

SA_CKE_0 SA_CKE_1 SB_CKE_0 SB_CKE_1 → M_CKE0 7,9, M_CKE1 7,9, M_CKE2 8,9, M_CKE3 8,9

SA_CS#_0 SA_CS#_1 SB_CS#_0 SB_CS#_1 → M_CS#0 7,9, M_CS#1 7,9, M_CS#2 8,9, M_CS#3 8,9

SA_ODT_0 SA_ODT_1 SB_ODT_0 SB_ODT_1 → M_ODT0 7,9, M_ODT1 7,9, M_ODT2 8,9, M_ODT3 8,9

SM_RCOMP M_RCOMP — R1112 2 80.6Ohm 1%
SM_RCOMP# M_RCOMP# — R1117 80.6Ohm 1%

+1.8V

SM_RCOMP_VOH SM_RCOMP_VOL

SM_VREF SM_PWROK SM_REXT SM_DRAMRST# — MCH_SM_REXT 499Ohm R1121 1%

M_VREF_MCH

C1105 0.01UF/50V /X

## CLK

DPLL_REF_CLK DPLL_REF_CLK# DPLL_REF_SSCLK DPLL_REF_SSCLK#

CLK_MCH_REF 29
CLK_MCH_REF# 29
CLK_MCH_SSCLK 29
CLK_MCH_SSCLK# 29

PEG_CLK PEG_CLK#

CLK_MCH_3GPLL 29
CLK_MCH_3GPLL# 29

## DMI

DMI_RXN_0 DMI_RXN_1 DMI_RXN_2 DMI_RXN_3 → DMI_TXN0 21, DMI_TXN1 21, DMI_TXN2 21, DMI_TXN3 21

DMI_RXP_0 DMI_RXP_1 DMI_RXP_2 DMI_RXP_3 → DMI_TXP0 21, DMI_TXP1 21, DMI_TXP2 21, DMI_TXP3 21

DMI_TXN_0 DMI_TXN_1 DMI_TXN_2 DMI_TXN_3 → DMI_RXN0 21, DMI_RXN1 21, DMI_RXN2 21, DMI_RXN3 21

DMI_TXP_0 DMI_TXP_1 DMI_TXP_2 DMI_TXP_3 → DMI_RXP0 21, DMI_RXP1 21, DMI_RXP2 21, DMI_RXP3 21

## CFG

29 MCH_BSEL0
29 MCH_BSEL1
29 MCH_BSEL2
T1102 MCH_CFG_3
T1101 MCH_CFG_4
16 MCH_CFG_5
16 MCH_CFG_6
16 MCH_CFG_7
T1115 MCH_CFG_8
16 MCH_CFG_9
16 MCH_CFG_10
T1107 MCH_CFG_11
16 MCH_CFG_12
16 MCH_CFG_13
T1103 MCH_CFG_14
T1108 MCH_CFG_15
16 MCH_CFG_16
T1104 MCH_CFG_17
T1109 MCH_CFG_18
16 MCH_CFG_19
16 MCH_CFG_20

CFG_0 … CFG_20

## GRAPHICS VID

GFX_VID_0 GFX_VID_1 GFX_VID_2 GFX_VID_3 GFX_VID_4

B33 GFX_VID_0 — T1110
B32 GFX_VID_1 — T1111
G33 GFX_VID_2 — T1112
F33 GFX_VID_3 — T1113
E33 GFX_VID_4 — T1114

GFX_VR_EN C34 GFX_VR_EN — T1106

## PM

22 PMSYNC# — RX1103 0Ohm PMSYNC# MCH — R29
3,20,78 H_DPRSTP# — B7
PM_EXTTS#0 N33
PM_EXTTS#1 P32
3,22,30 PM_PWROK — RX1102 0Ohm — PM_PWROK_MCH AT40
5,21,30,33,43,53,62 BUF_PLT_RST# — BUF_PLT_RST# MCH AT11
3,5,20,31 H_THRMTRIP# — RX1101 100Ohm — T20
22,78 PM_DPRSLPVR — RX1104 0Ohm — PM_DPRSLPVR_MCH R32

PM_SYNC#
PM_DPRSTP#
PM_EXT_TS#_0
PM_EXT_TS#_1
PWROK
RSTIN#
THERMTRIP#
DPRSLPVR

## ME

CL_CLK CL_DATA CL_PWROK CL_RST# CL_VREF

AH37 CL_CLK0 — 22
AH36 CL_DATA0 — 22
AN36
AJ35 CL_RST#0 — 22
AH34 CL_VREF

11/02
PM_PWROK_MCH
CL_VREF

C1106 0.1UF/16V

R1108 1KOhm 1%
R1102 499Ohm 1%

+VCCP

## MISC

DDPC_CTRLCLK DDPC_CTRLDATA SDVO_CTRLCLK SDVO_CTRLDATA CLKREQ# ICH_SYNC#

N28 DDPC_CTRLCLK — T1118
M28 DDPC_CTRLDATA
G36 HDMI_SCL — HDMI_SCL 48
E36 HDMI_SDA — HDMI_SDA 48
K36 MCH_CLKREQ#
H36 MCH_ICH_SYNC# — 22

TSATN#

T1117
B12 TSATN# — R1126 56Ohm

+VCCP

## HDA

HDA_BCLK HDA_RST# HDA_SDI HDA_SDO HDA_SYNC

B28 ACZ_BCLK_NB_R 49
B30 ACZ_RST#_NB_R 49
B29 R1174 33Ohm ACZ_SDIN2_R 49
C29 ACZ_SDOUT_NB_R 49
A28 ACZ_SYNC_NB_R 49

For HDMI

## NC

BG48 BF48 BD48 BC48 BH47 BG47 BE47 BH46 BF46 BG45 BH44 BH43 BH6 BH5 BG4 BH3 BF3 BH2 BG2 BE2 BG1 BF1 BD1 BC1 F1

NC_1 … NC_25

CANTIGA_CHIPSET

---

+1.8V

R1105 1KOhm 1%
SM_RCOMP_VOH
C1101 2.2UF/10V
C1102 0.01UF/50V
R1106 3.01KOHM
SM_RCOMP_VOL
R1107 1KOhm 1%
C1103 2.2UF/10V
C1104 0.01UF/50V

+3VS

R1103 10KOhm — PM_EXTTS#0 7
R1104 10KOhm — PM_EXTTS#1 8
R1111 N/A 10KOhm — MCH_CLKREQ#

+1.8V

R1109 1KOhm 1% N/A — M_VREF_MCH 7,8
R1110 1KOhm 1% N/A
C1107 0.1UF/16V
GND GND

2008-07-16

**SDVO_CTRL_DATA : SDVO/iHDMI/DP Interface Present**

0 = SDVO/iHDMI/DP Disabled (D)
1 = SDVO/iHDMI/DP Enabled

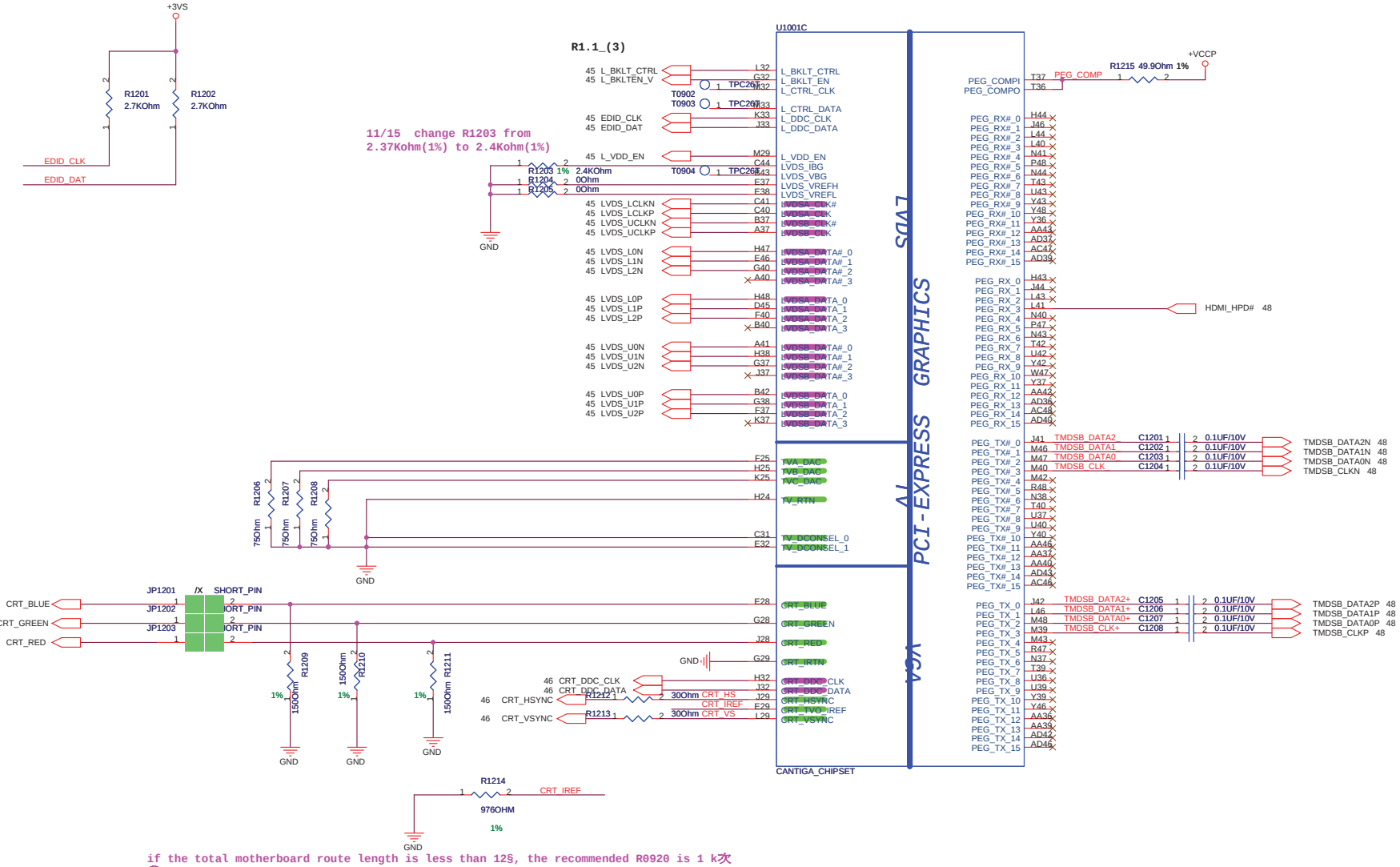
+3VS
HDMI_SDA — R1149 /X 4.02KOHM 1%

**DDPC_CTRL_DATA : SDVO/iHDMI/DP Device Present**

0 = No SDVO/iHDMI/DP (D)
1 = SDVO/iHDMI/DP Present

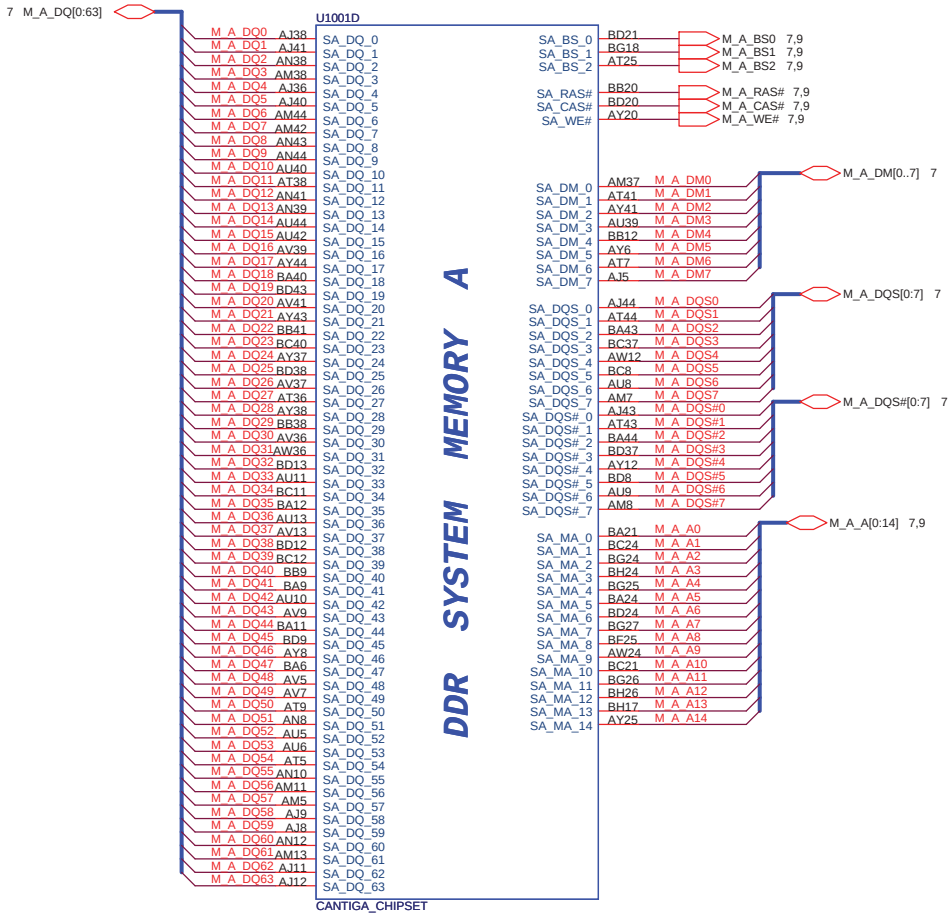
+3VS
DDPC_CTRLDATA — R1150 /X 4.02KOHM 1%

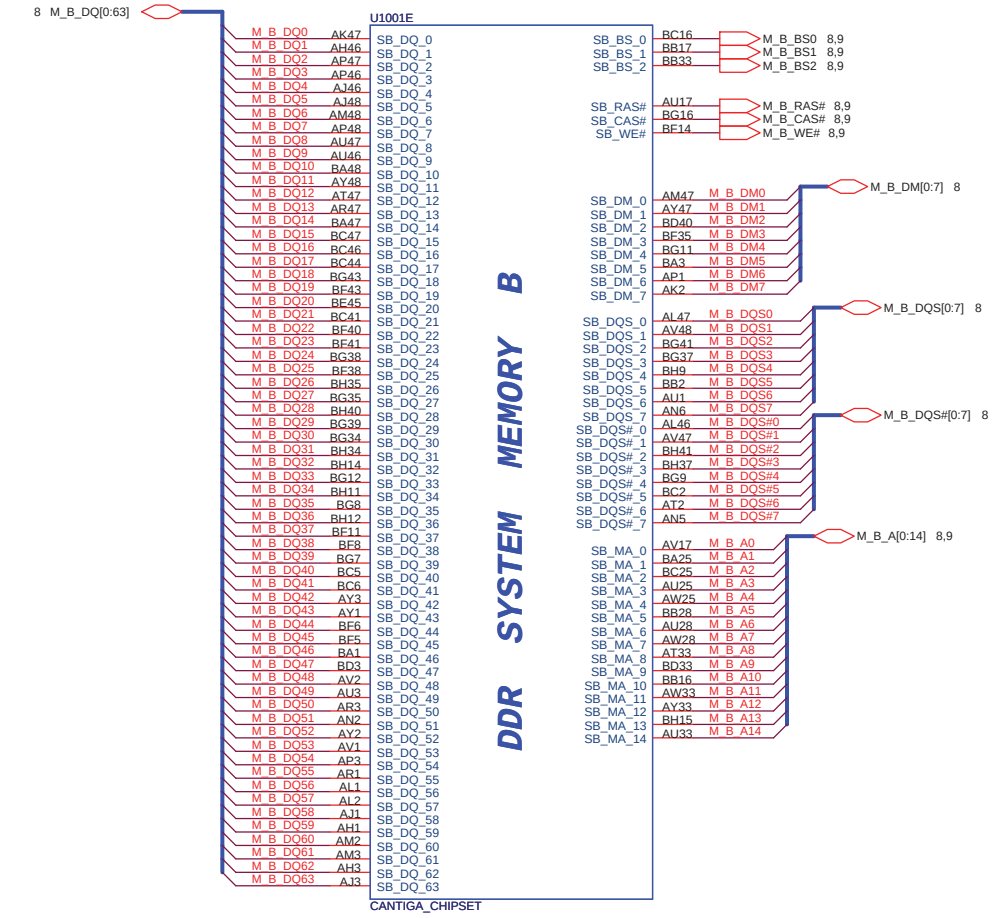
| | |
|---|---|
| Title | Cantiga-DDR2/PEG(2) |
| ASUSTeK COMPUTER INC. NB1 | Engineer: yun-feng_yan |
| Size: Custom | Project Name: N50A/N51A |
| Rev | 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 11 of 79 |





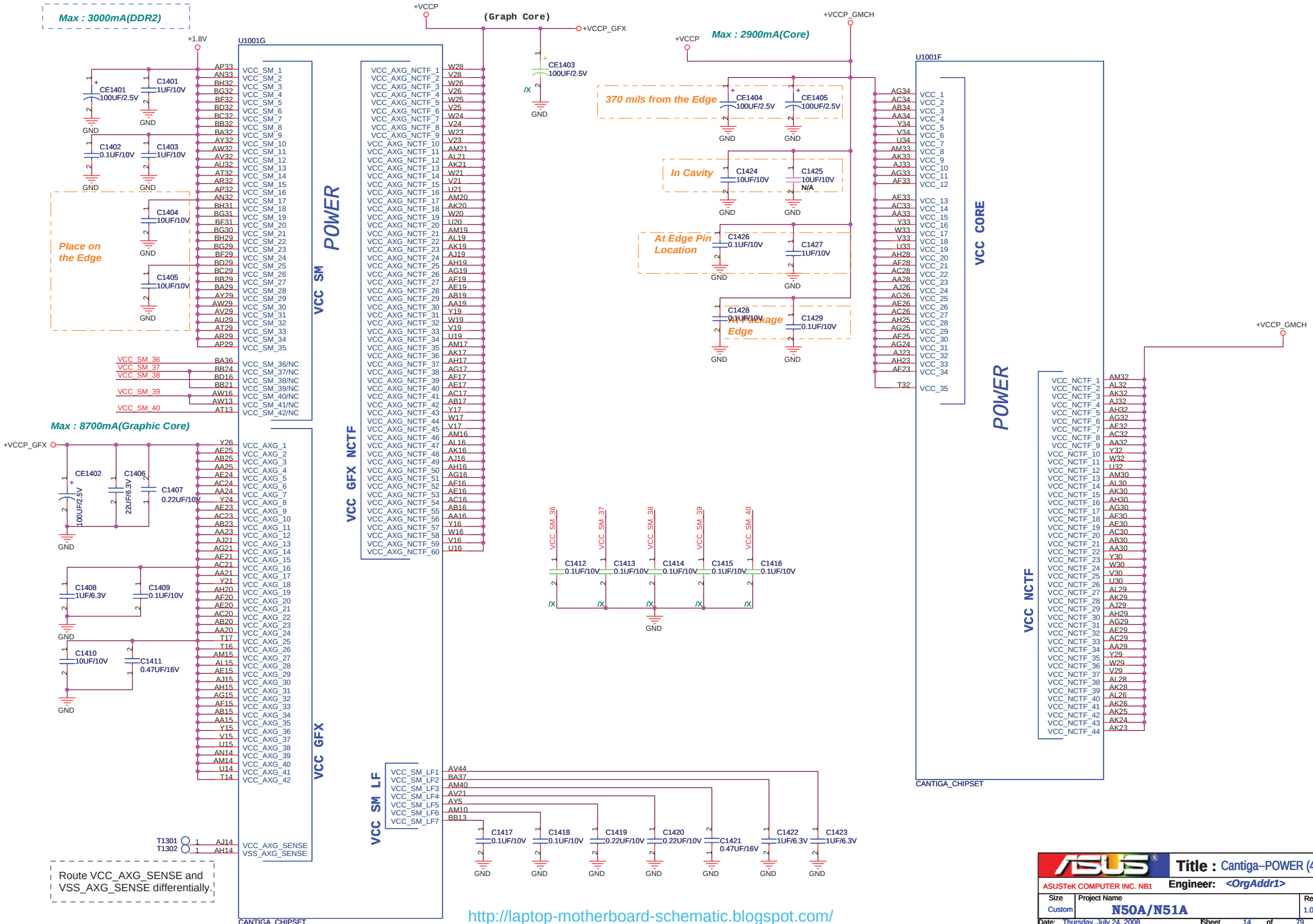

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : | |
| | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 12 of 79 | |

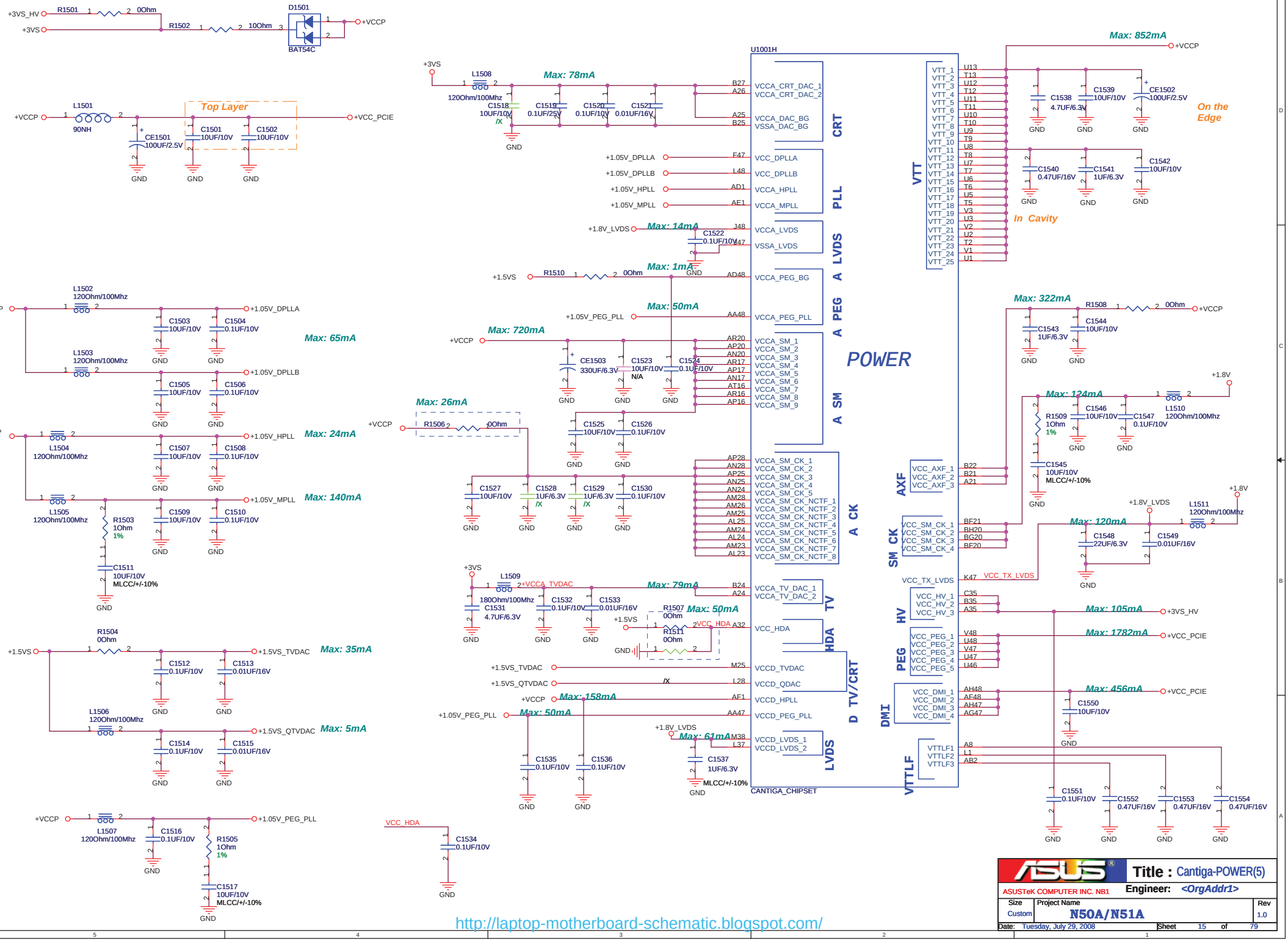


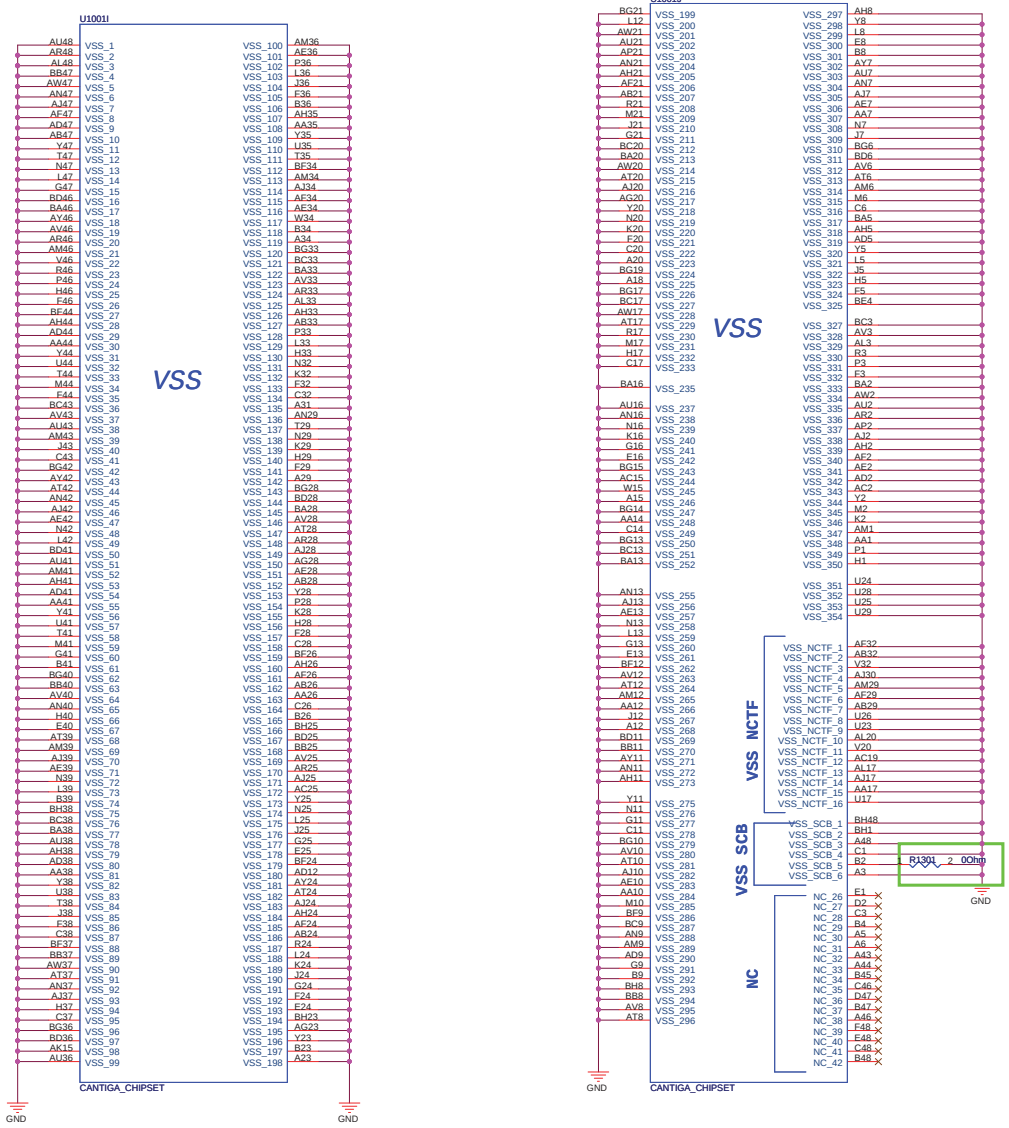





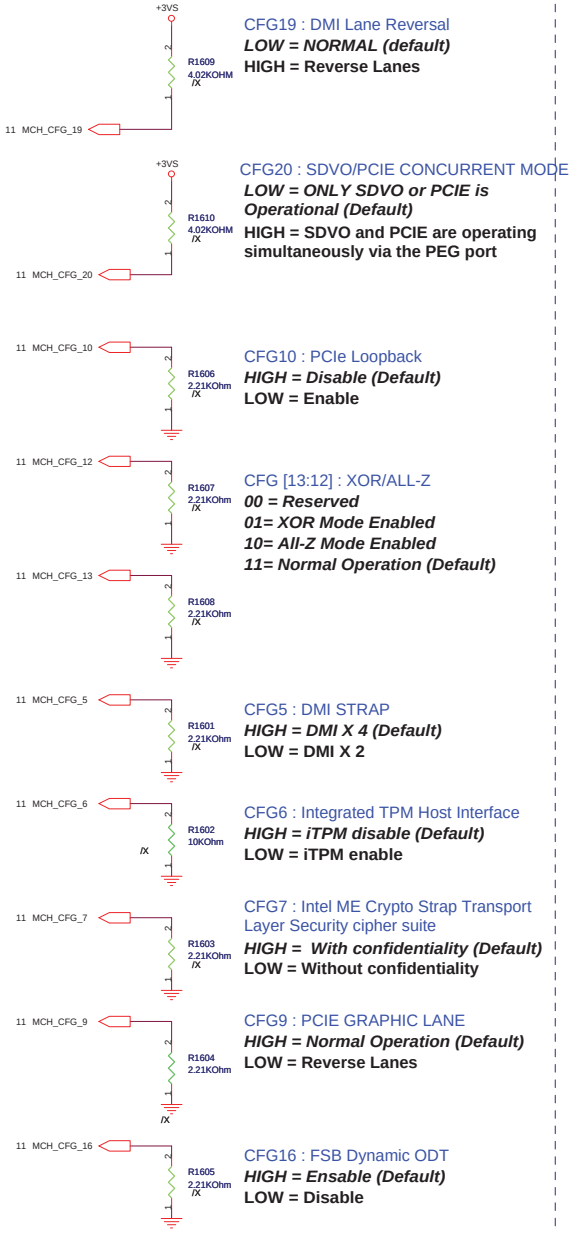

| | | |
|---|---|---|
| Title : Cantiga--DDR2 bus (3) | | |
| ASUSTeK COMPUTER INC. NB1 | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Friday, August 01, 2008 | Sheet 13 of 79 | |


Max : 3000mA(DDR2)
+1.8V
U1001G
VCC_SM_1
VCC_SM_2
VCC_SM_3
VCC_SM_4
VCC_SM_5
VCC_SM_6
VCC_SM_7
VCC_SM_8
VCC_SM_9
VCC_SM_10
VCC_SM_11
VCC_SM_12
VCC_SM_13
VCC_SM_14
VCC_SM_15
VCC_SM_16
VCC_SM_17
VCC_SM_18
VCC_SM_19
VCC_SM_20
VCC_SM_21
VCC_SM_22
VCC_SM_23
VCC_SM_24
VCC_SM_25
VCC_SM_26
VCC_SM_27
VCC_SM_28
VCC_SM_29
VCC_SM_30
VCC_SM_31
VCC_SM_32
VCC_SM_33
VCC_SM_34
VCC_SM_35
VCC_SM_36/NC
VCC_SM_37/NC
VCC_SM_38/NC
VCC_SM_39/NC
VCC_SM_40/NC
VCC_SM_41/NC
VCC_SM_42/NC
VCC SM POWER
CE1401 100UF/2.5V
C1401 1UF/10V
C1402 0.1UF/10V
C1403 1UF/10V
C1404 10UF/10V
C1405 10UF/10V
Place on the Edge
GND
Max : 8700mA(Graphic Core)
+VCCP_GFX
VCC_AXG_1
VCC_AXG_2
VCC_AXG_3
VCC_AXG_4
VCC_AXG_5
VCC_AXG_6
VCC_AXG_7
VCC_AXG_8
VCC_AXG_9
VCC_AXG_10
VCC_AXG_11
VCC_AXG_12
VCC_AXG_13
VCC_AXG_14
VCC_AXG_15
VCC_AXG_16
VCC_AXG_17
VCC_AXG_18
VCC_AXG_19
VCC_AXG_20
VCC_AXG_21
VCC_AXG_22
VCC_AXG_23
VCC_AXG_24
VCC_AXG_25
VCC_AXG_26
VCC_AXG_27
VCC_AXG_28
VCC_AXG_29
VCC_AXG_30
VCC_AXG_31
VCC_AXG_32
VCC_AXG_33
VCC_AXG_34
VCC_AXG_35
VCC_AXG_36
VCC_AXG_37
VCC_AXG_38
VCC_AXG_39
VCC_AXG_40
VCC_AXG_41
VCC_AXG_42
VCC_AXG_SENSE
VSS_AXG_SENSE
VCC GFX
CE1402 100UF/2.5V
C1406 22UF/6.3V
C1407 0.22UF/10V
C1408 1UF/6.3V
C1409 0.1UF/10V
C1410 10UF/10V
C1411 0.47UF/16V
T1301
T1302
Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially.
+VCCP
(Graph Core)
+VCCP_GFX
CE1403 100UF/2.5V
VCC_AXG_NCTF_1
VCC_AXG_NCTF_2
VCC_AXG_NCTF_3
VCC_AXG_NCTF_4
VCC_AXG_NCTF_5
VCC_AXG_NCTF_6
VCC_AXG_NCTF_7
VCC_AXG_NCTF_8
VCC_AXG_NCTF_9
VCC_AXG_NCTF_10
VCC_AXG_NCTF_11
VCC_AXG_NCTF_12
VCC_AXG_NCTF_13
VCC_AXG_NCTF_14
VCC_AXG_NCTF_15
VCC_AXG_NCTF_16
VCC_AXG_NCTF_17
VCC_AXG_NCTF_18
VCC_AXG_NCTF_19
VCC_AXG_NCTF_20
VCC_AXG_NCTF_21
VCC_AXG_NCTF_22
VCC_AXG_NCTF_23
VCC_AXG_NCTF_24
VCC_AXG_NCTF_25
VCC_AXG_NCTF_26
VCC_AXG_NCTF_27
VCC_AXG_NCTF_28
VCC_AXG_NCTF_29
VCC_AXG_NCTF_30
VCC_AXG_NCTF_31
VCC_AXG_NCTF_32
VCC_AXG_NCTF_33
VCC_AXG_NCTF_34
VCC_AXG_NCTF_35
VCC_AXG_NCTF_36
VCC_AXG_NCTF_37
VCC_AXG_NCTF_38
VCC_AXG_NCTF_39
VCC_AXG_NCTF_40
VCC_AXG_NCTF_41
VCC_AXG_NCTF_42
VCC_AXG_NCTF_43
VCC_AXG_NCTF_44
VCC_AXG_NCTF_45
VCC_AXG_NCTF_46
VCC_AXG_NCTF_47
VCC_AXG_NCTF_48
VCC_AXG_NCTF_49
VCC_AXG_NCTF_50
VCC_AXG_NCTF_51
VCC_AXG_NCTF_52
VCC_AXG_NCTF_53
VCC_AXG_NCTF_54
VCC_AXG_NCTF_55
VCC_AXG_NCTF_56
VCC_AXG_NCTF_57
VCC_AXG_NCTF_58
VCC_AXG_NCTF_59
VCC_AXG_NCTF_60
VCC GFX NCTF
VCC_SM_36
VCC_SM_37
VCC_SM_38
VCC_SM_39
VCC_SM_40
C1412 0.1UF/10V
C1413 0.1UF/10V
C1414 0.1UF/10V
C1415 0.1UF/10V
C1416 0.1UF/10V
VCC_SM_LF1
VCC_SM_LF2
VCC_SM_LF3
VCC_SM_LF4
VCC_SM_LF5
VCC_SM_LF6
VCC_SM_LF7
VCC SM LF
C1417 0.1UF/10V
C1418 0.1UF/10V
C1419 0.22UF/10V
C1420 0.22UF/10V
C1421 0.47UF/16V
C1422 1UF/6.3V
C1423 1UF/6.3V
CANTIGA_CHIPSET
+VCCP
Max : 2900mA(Core)
+VCCP_GMCH
370 mils from the Edge
CE1404 100UF/2.5V
CE1405 100UF/2.5V
In Cavity
C1424 10UF/10V
C1425 10UF/10V N/A
At Edge Pin Location
C1426 0.1UF/10V
C1427 1UF/10V
C1428 0.1UF/10V
C1429 0.1UF/10V
At Package Edge
U1001F
VCC_1
VCC_2
VCC_3
VCC_4
VCC_5
VCC_6
VCC_7
VCC_8
VCC_9
VCC_10
VCC_11
VCC_12
VCC_13
VCC_14
VCC_15
VCC_16
VCC_17
VCC_18
VCC_19
VCC_20
VCC_21
VCC_22
VCC_23
VCC_24
VCC_25
VCC_26
VCC_27
VCC_28
VCC_29
VCC_30
VCC_31
VCC_32
VCC_33
VCC_34
VCC_35
VCC CORE
POWER
+VCCP_GMCH
VCC_NCTF_1
VCC_NCTF_2
VCC_NCTF_3
VCC_NCTF_4
VCC_NCTF_5
VCC_NCTF_6
VCC_NCTF_7
VCC_NCTF_8
VCC_NCTF_9
VCC_NCTF_10
VCC_NCTF_11
VCC_NCTF_12
VCC_NCTF_13
VCC_NCTF_14
VCC_NCTF_15
VCC_NCTF_16
VCC_NCTF_17
VCC_NCTF_18
VCC_NCTF_19
VCC_NCTF_20
VCC_NCTF_21
VCC_NCTF_22
VCC_NCTF_23
VCC_NCTF_24
VCC_NCTF_25
VCC_NCTF_26
VCC_NCTF_27
VCC_NCTF_28
VCC_NCTF_29
VCC_NCTF_30
VCC_NCTF_31
VCC_NCTF_32
VCC_NCTF_33
VCC_NCTF_34
VCC_NCTF_35
VCC_NCTF_36
VCC_NCTF_37
VCC_NCTF_38
VCC_NCTF_39
VCC_NCTF_40
VCC_NCTF_41
VCC_NCTF_42
VCC_NCTF_43
VCC_NCTF_44
VCC NCTF
CANTIGA_CHIPSET
http://laptop-motherboard-schematic.blogspot.com/
Title : Cantiga--POWER (4)
ASUSTeK COMPUTER INC. NB1
Engineer: <OrgAddr1>
Size Custom
Project Name N50A/N51A
Rev 1.0
Date: Thursday, July 24, 2008
Sheet 14 of 79


+3VS_HV
R1501 0Ohm
+3VS
R1502 10Ohm
D1501
BAT54C
+VCCP
L1501
90NH
Top Layer
+VCC_PCIE
CE1501 100UF/2.5V
C1501 10UF/10V
C1502 10UF/10V
GND
U1001H
CANTIGA_CHIPSET
POWER
CRT
PLL
LVDS
PEG
SM CK
TV
HDA
DMI
VTTLF
VTT
AXF
Max: 852mA
Max: 78mA
Max: 14mA
Max: 1mA
Max: 50mA
Max: 720mA
Max: 26mA
Max: 65mA
Max: 24mA
Max: 140mA
Max: 35mA
Max: 5mA
Max: 322mA
Max: 124mA
Max: 120mA
Max: 79mA
Max: 158mA
Max: 61mA
Max: 105mA
Max: 1782mA
Max: 456mA
On the Edge
In Cavity
http://laptop-motherboard-schematic.blogspot.com/
Title : Cantiga-POWER(5)
ASUSTeK COMPUTER INC. NB1
Engineer: <OrgAddr1>
Size Custom
Project Name N50A/N51A
Rev 1.0
Date: Tuesday, July 29, 2008
Sheet 15 of 79




R1.1_(4)






ASUSTeK COMPUTER INC. NB1

Title : Cantiga-GND

Engineer: <OrgAddr1>

| Size | Project Name | Rev |
|---|---|---|
| C | N50A/N51A | 1.0 |

Date: Friday, August 01, 2008 Sheet 16 of 79

| | |
|---|---|
| Title : | |
| ASUSTeK COMPUTER INC. NB1 | Engineer: <OrgAddr1> |
| Size: A | Project Name: N50A/N51A |
| Rev: 1.0 | |
| Date: Thursday, July 24, 2008 | Sheet 17 of 79 |

Title :

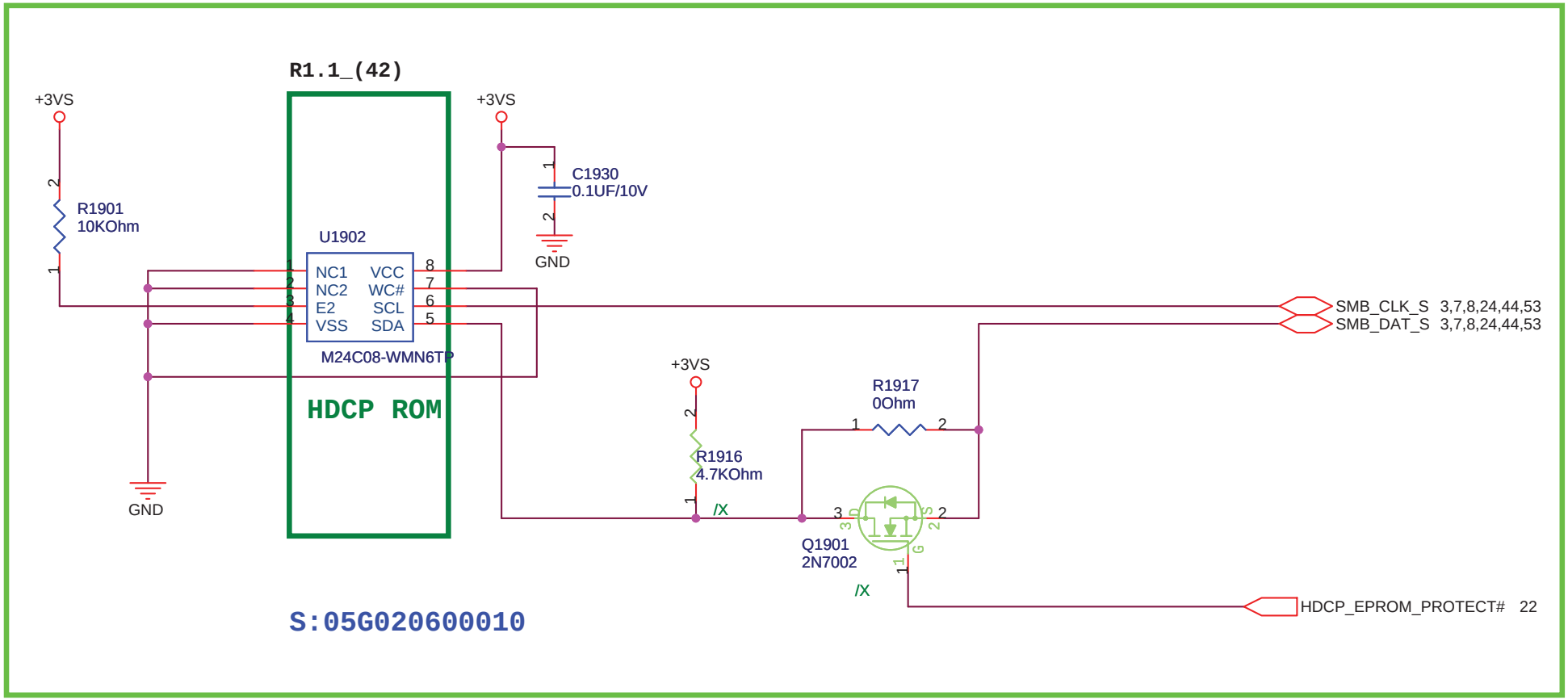
ASUSTeK COMPUTER INC. NB1

Engineer: <OrgAddr1>

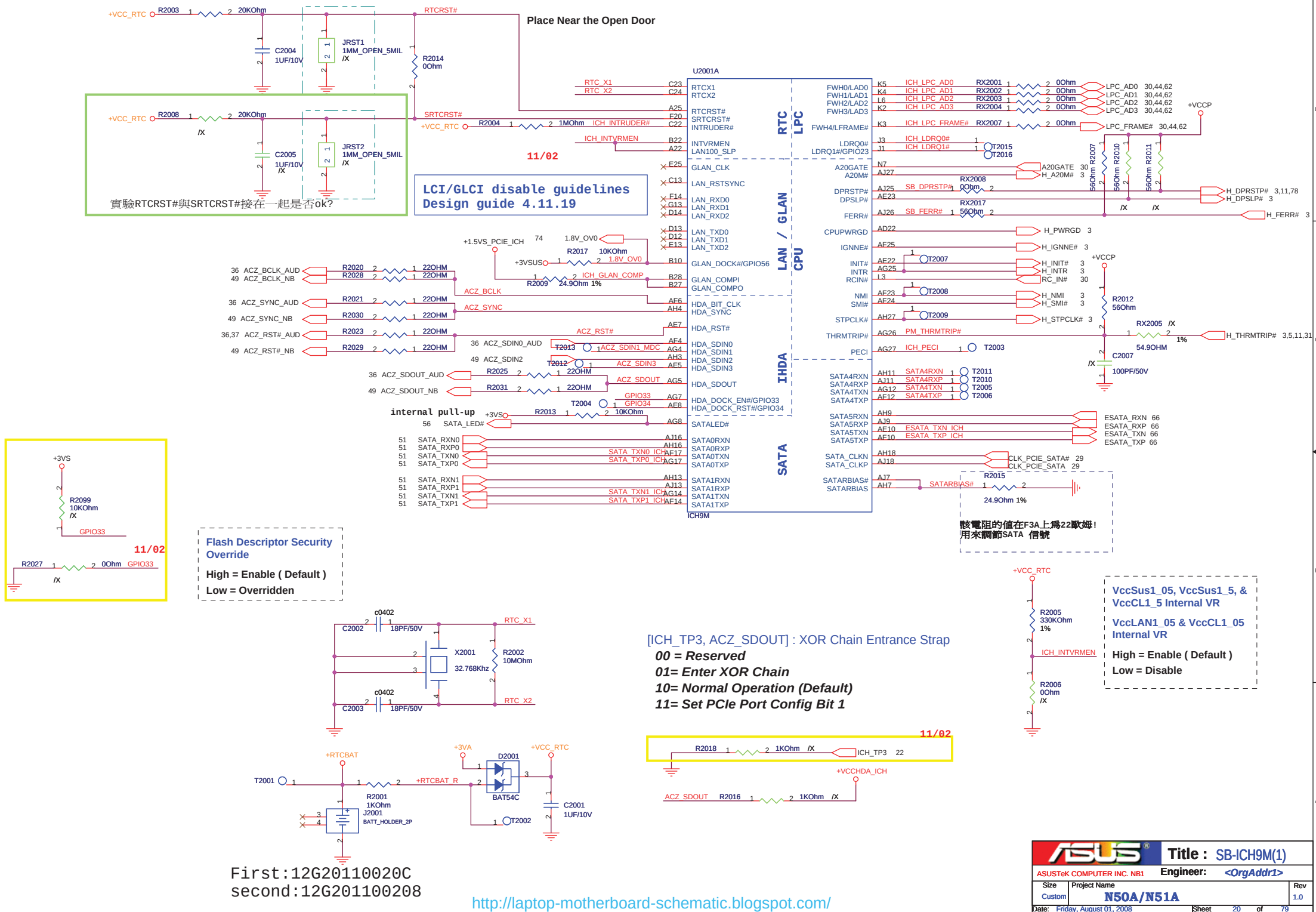
| Size | Project Name | Rev |
|---|---|---|
| B | N50A/N51A | 1.0 |

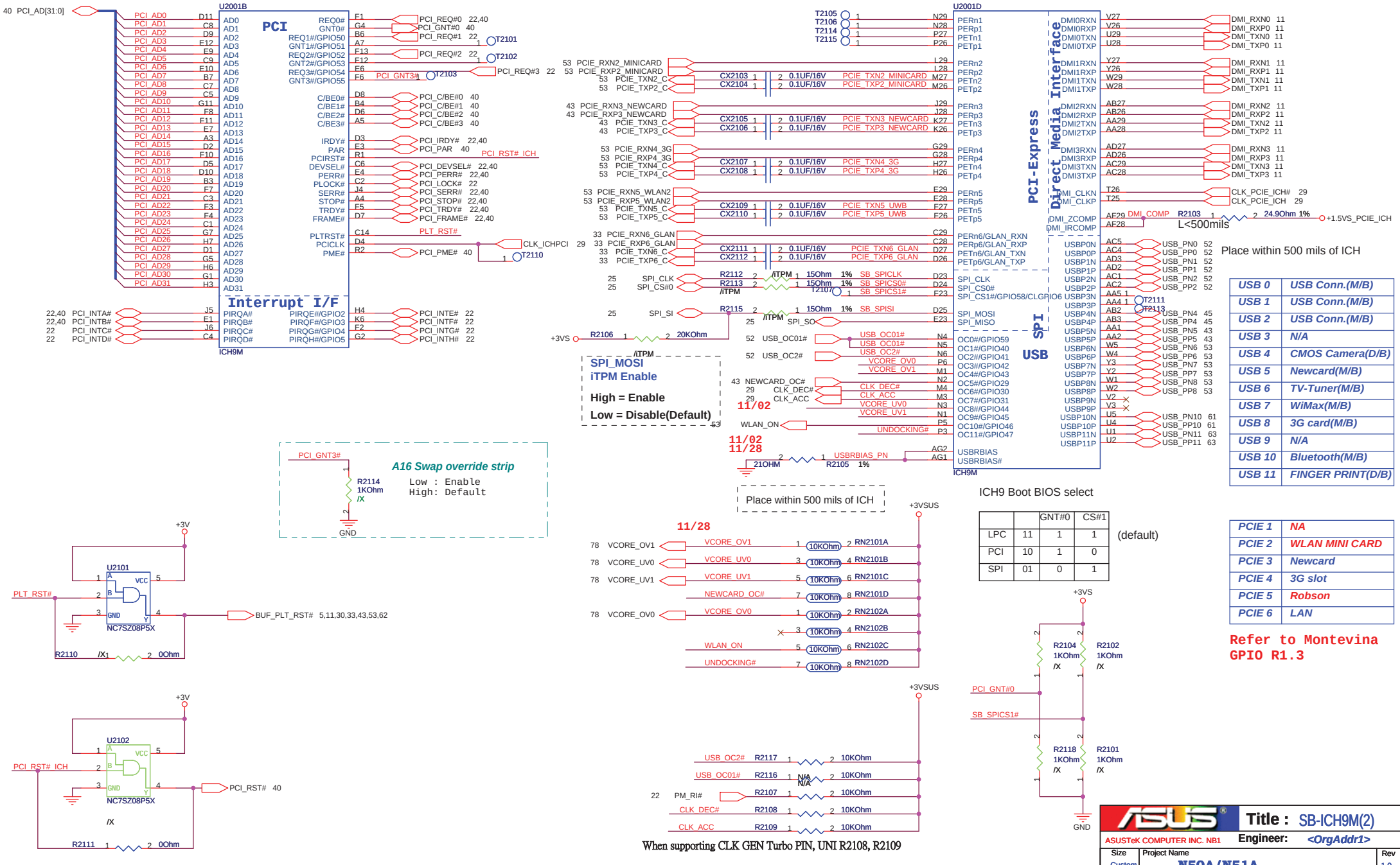
Date: Thursday, July 24, 2008 Sheet 18 of 79

R1.1_(11)




| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : | |
| | Engineer: <OrgAddr1> | |
| Size: A | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Friday, August 01, 2008 | Sheet 19 of 79 | |


Place Near the Open Door
11/02
實驗RTCRST#與SRTCRST#接在一起是否ok?
LCI/GLCI disable guidelines
Design guide 4.11.19
U2001A
ICH9M
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
internal pull-up
Flash Descriptor Security Override
High = Enable ( Default )
Low = Overridden
[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap
00 = Reserved
01= Enter XOR Chain
10= Normal Operation (Default)
11= Set PCIe Port Config Bit 1
11/02
R2018 1 2 1KOhm /X ICH_TP3 22
+VCCHDA_ICH
ACZ_SDOUT R2016 1 2 1KOhm /X
R2015
24.9Ohm 1%
駭電阻的值在F3A上爲22歐姆!
用來調節SATA 信號
VccSus1_05, VccSus1_5, & VccCL1_5 Internal VR
VccLAN1_05 & VccCL1_05 Internal VR
High = Enable ( Default )
Low = Disable
R2005 330KOhm 1%
R2006 0Ohm /X
X2001 32.768Khz
C2002 18PF/50V
C2003 18PF/50V
R2002 10MOhm
D2001 BAT54C
R2001 1KOhm
J2001 BATT_HOLDER_2P
C2001 1UF/10V
T2001
T2002
First:12G20110020C
second:12G201100208
http://laptop-motherboard-schematic.blogspot.com/
Title : SB-ICH9M(1)
ASUSTeK COMPUTER INC. NB1
Engineer: <OrgAddr1>
Size Custom
Project Name N50A/N51A
Rev 1.0
Date: Friday, August 01, 2008
Sheet 20 of 79

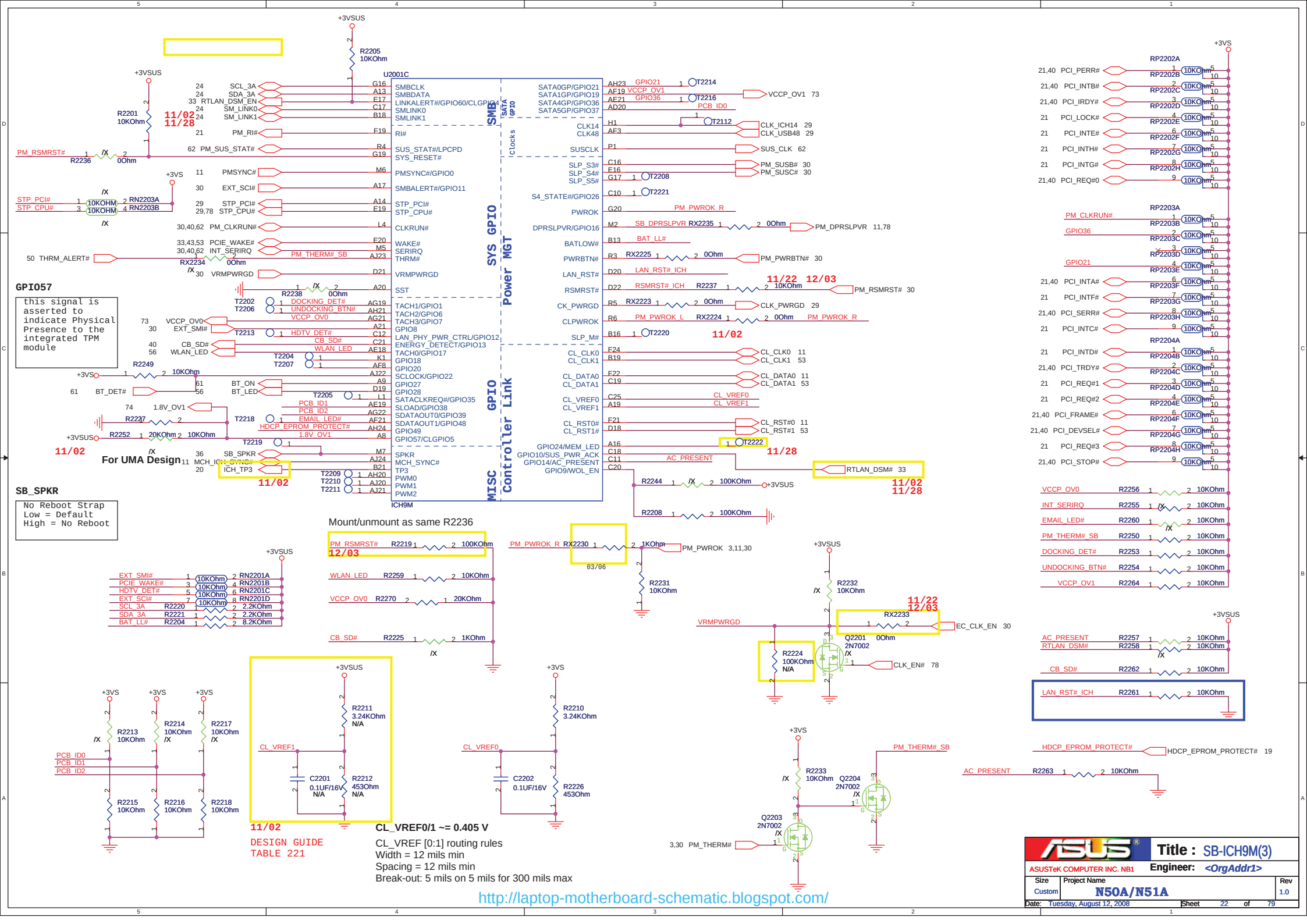


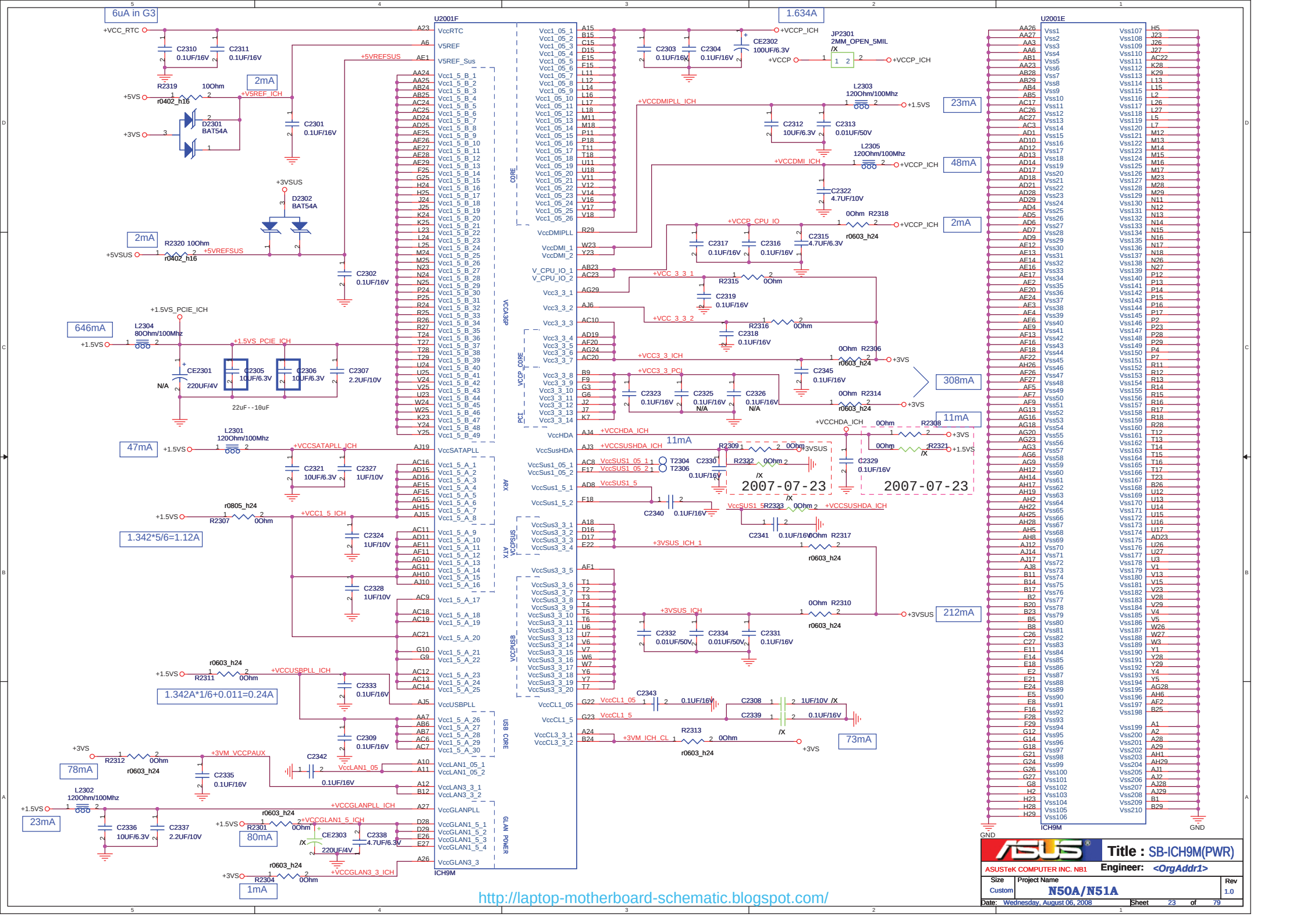

| | |
|---|---|
| USB 0 | USB Conn.(M/B) |
| USB 1 | USB Conn.(M/B) |
| USB 2 | USB Conn.(M/B) |
| USB 3 | N/A |
| USB 4 | CMOS Camera(D/B) |
| USB 5 | Newcard(M/B) |
| USB 6 | TV-Tuner(M/B) |
| USB 7 | WiMax(M/B) |
| USB 8 | 3G card(M/B) |
| USB 9 | N/A |
| USB 10 | Bluetooth(M/B) |
| USB 11 | FINGER PRINT(D/B) |

| | | GNT#0 | CS#1 |
|---|---|---|---|
| LPC | 11 | 1 | 1 |
| PCI | 10 | 1 | 0 |
| SPI | 01 | 0 | 1 |

| | |
|---|---|
| PCIE 1 | NA |
| PCIE 2 | WLAN MINI CARD |
| PCIE 3 | Newcard |
| PCIE 4 | 3G slot |
| PCIE 5 | Robson |
| PCIE 6 | LAN |

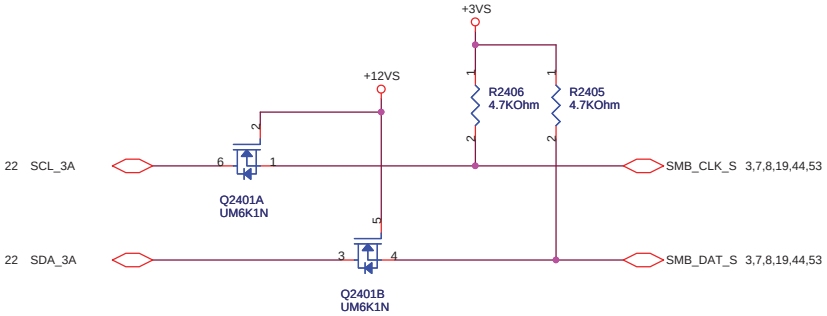
| | | | |
|---|---|---|---|
| Title : | SB-ICH9M(2) | | |
| ASUSTeK COMPUTER INC. NB1 | Engineer: | <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 21 of 79 | | |

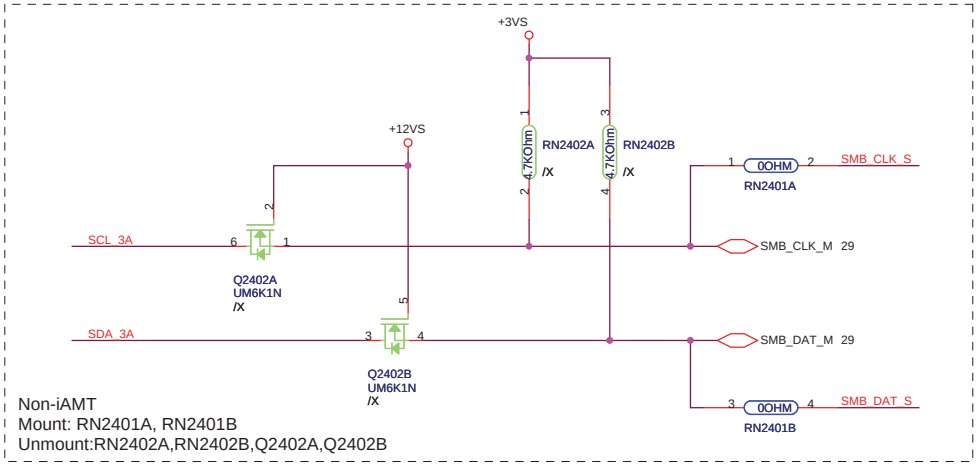

U2001C
ICH9M
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STP_PCI#
STP_CPU#
CLKRUN#
WAKE#
SERIRQ
THRM#
VRMPWRGD
SST
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
ENERGY_DETECT/GPIO13
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
PWM0
PWM1
PWM2
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_RST1#
GPIO24/MEM_LED
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
GPIO9/WOL_EN
GPIO57
this signal is asserted to indicate Physical Presence to the integrated TPM module
SB_SPKR
No Reboot Strap
Low = Default
High = No Reboot
For UMA Design
Mount/unmount as same R2236
DESIGN GUIDE TABLE 221
CL_VREF0/1 ~= 0.405 V
CL_VREF [0:1] routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out: 5 mils on 5 mils for 300 mils max
http://laptop-motherboard-schematic.blogspot.com/
Title : SB-ICH9M(3)
ASUSTeK COMPUTER INC. NB1
Engineer: <OrgAddr1>
Size: Custom
Project Name: N50A/N51A
Rev: 1.0
Date: Tuesday, August 12, 2008
Sheet 22 of 79



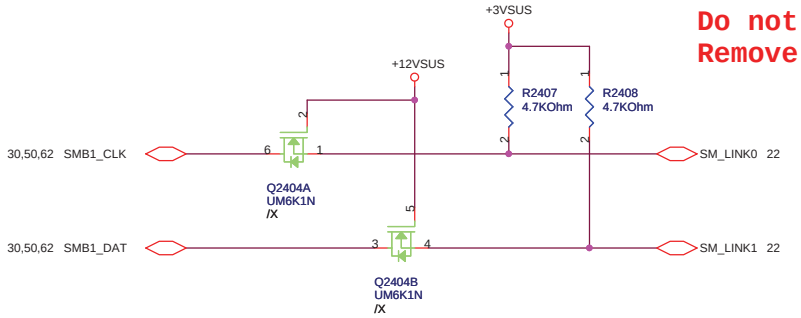

| | | | |
|---|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Engineer: <OrgAddr1> | Title : SB-ICH9M(PWR) | |
| Size: Custom | Project Name: N50A/N51A | | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 23 of 79 | | |

## ICH9-M




## EC-IT8752

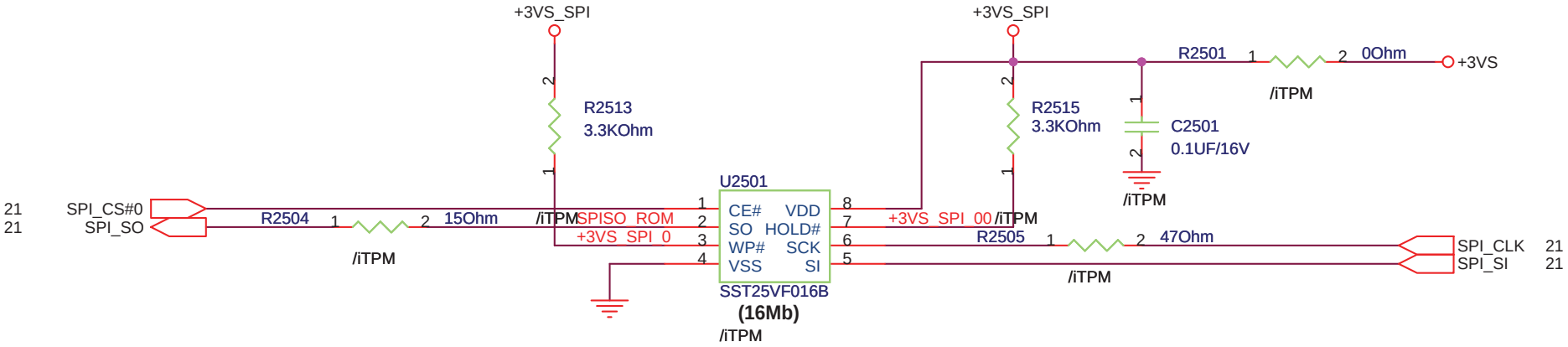



**Do not support iAMT**
**Remove ME-EC smbus**

| Master | Slave |
|---|---|
| SCL_3A<br>SDA_3A<br>(ICH9M) | A. SMB_CLK_S<br>SMB_DAT_S → SO-DIMM0; SO-DIMM1; Debug; WLAN Card<br>B. SMB_CLK_M<br>SMB_DAT_M → CLK Generator |
| SMB0_CLK<br>SMB0_DAT<br>(EC) | BATTERY |
| SMB1_CLK<br>SMB1_DAT<br>(EC) | Thermal Sensor |



| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : ICH9M-Other | |
| | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Friday, August 01, 2008 | Sheet 24 of 79 | |




# FOR iTPM
# 8Mb 05G00120A010

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : SPI ROM | |
| | Engineer: <OrgAddr1> | |
| Size: A | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 25 of 79 | |

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : | |
| | Engineer: <OrgAddr1> | |
| Size: A | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Thursday, July 24, 2008 | Sheet 26 of 79 | |

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : | |
| | Engineer: <OrgAddr1> | |
| Size: A | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Thursday, July 24, 2008 | Sheet 27 of 79 | |

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : | |
| | Engineer: <OrgAddr1> | |
| Size: A | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Thursday, July 24, 2008 | Sheet 28 of 79 | |

2 source:RTM875T-363 06G011501020

U2901

ICS9LPR363EGLF-T

## PEREQ#1
0: Enable control SATACLK & PCIEX0 / 6 through I2C
1: Disable SATACLK & PCIEX0 / 6 Controlled

## PEREQ#2
0: Enable control PCIEX 1 / 8 through I2C
1: Disable PCIEX1/8 Controlled

## PEREQ#3
0: Enable control PCIEX 4 / 2 through I2C
1: Disable PCIEX 4 / 2 Controlled

## PEREQ#4
0: Enable control PCIEX 7 / 5 / 3 through I2C
1: Disable PCIEX 7 / 5 / 3 Controlled

## Latched Input Select

**Decide pin 43/44**
0 = SRC CLK
1 = CPU_ITP CLK
(Pin8)
ITP_EN

**Decide pin 17/18**
0 = LCDCLK
1 = PCIEX
(Pin5)
SELPCIE0_LCD#

**Decide pin 40/41**
0 = PCIECLK
1 = PEREQ#
(Pin64)
REQ_SEL#

**Decide pin 17/18**
SELLCD_27# = 0:
pin14/15=PCIEX_9L
pin17/18=27FIX/27SS
SELLCD_27# = 1:
pin14/15=DOT_96MHzL
pin17/18=LCD_SSCG/PCIe_L0
(Pin9)

| | FSLC | FSLB | FSLA |
|---|---|---|---|
| BCLK | BSEL2 | BSEL1 | BSEL0 |
| 166 | 0 | 1 | 1 |
| 200 | 0 | 1 | 0 |
| 266 | 0 | 0 | 0 |

| | R2902 | R2903 | R2920 |
|---|---|---|---|
| 363: VREF | 1K | 330 | UNI |
| 364: TURBO | UNI | 10K | 0 |
| 364:NO TBO | UNI | UNI | UNI |

Int PU/PD R=120K ohm.
Int PU: pin 5,9,32,33,34
Ext PD: pin 64

| Pin5 | Pin9 | Pin14/15 | Pin17/18 |
|---|---|---|---|
| SELPCIEX0_LCD#/ PCI3 = 0 (low) | SELLCD_27#=0 | PCIEX9 | 27FIXSS |
| | SELLCD_27#=1 | DOT96 | LCD |
| SELPCIEX0_LCD#/ PCI3 = 1 (high) | SELLCD_27#=0 | PCIEX9 | PCIEX0 |
| | SELLCD_27#=1 | DOT96 | PCIEX0 |

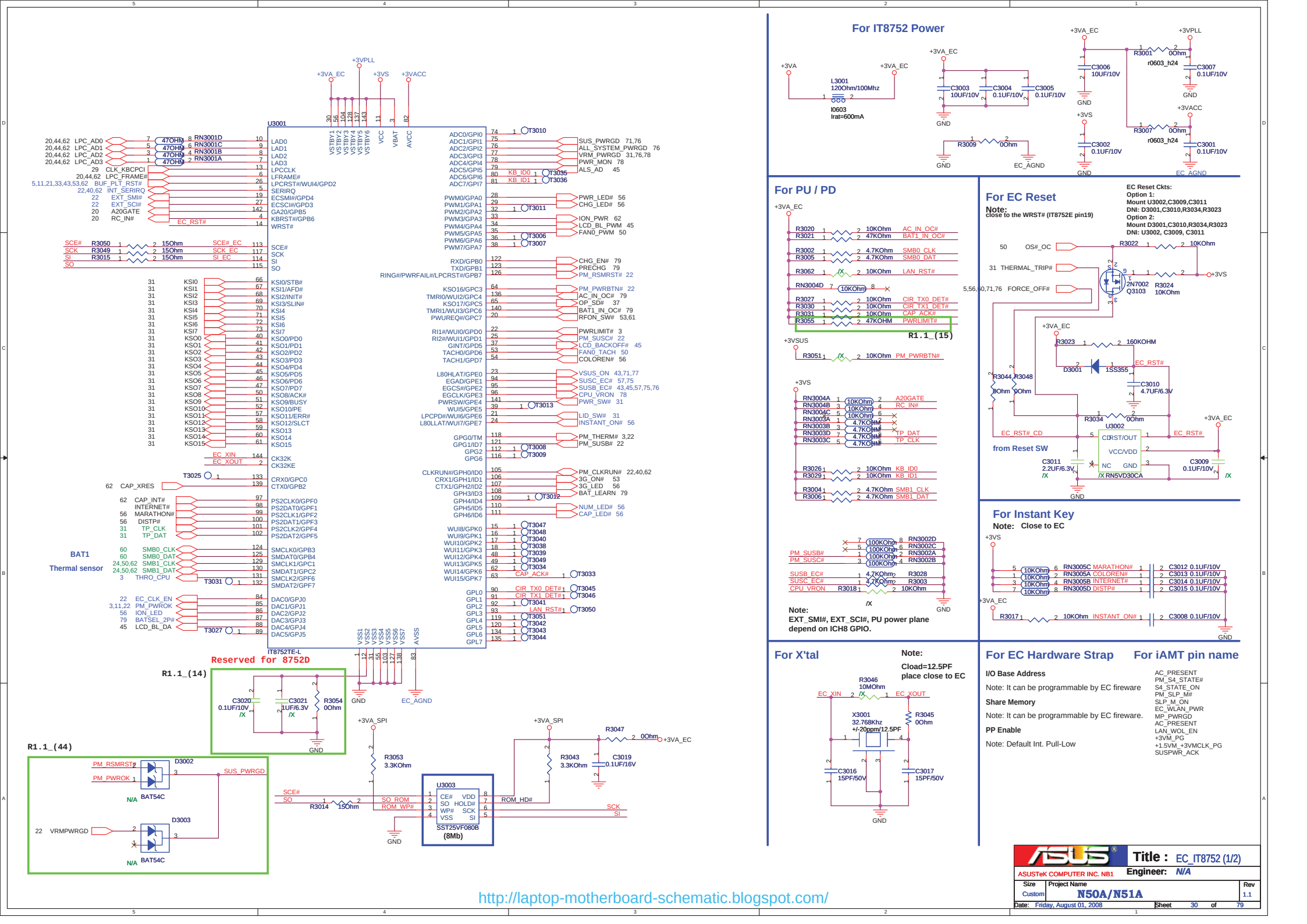
ASUSTeK COMPUTER INC. NB1

Title : CLOCK GEN

Engineer: <OrgAddr1>

Size: Custom | Project Name: N50A/N51A | Rev: 1.0

Date: Tuesday, August 05, 2008 | Sheet 29 of 79


For IT8752 Power
For PU / PD
For EC Reset
For Instant Key
For X'tal
For EC Hardware Strap
For iAMT pin name
U3001
IT8752TE-L
Reserved for 8752D
BAT1
Thermal sensor
U3003
SST25VF080B
(8Mb)
Title : EC_IT8752 (1/2)
ASUSTeK COMPUTER INC. NB1
Engineer: N/A
Project Name N50A/N51A
Rev 1.1
Date: Friday, August 01, 2008
Sheet 30 of 79
http://laptop-motherboard-schematic.blogspot.com/

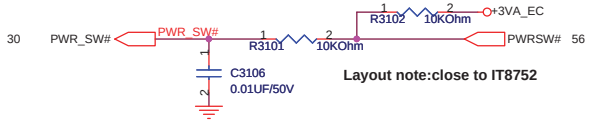
## For Battery

**Note:** When plug in or out the battery, it may cause a spike to damage EC and gas gauge. It needs to add varistors to protect those pins.

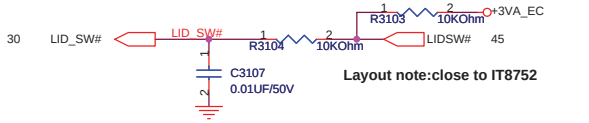
# In Page 60

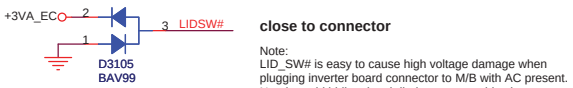
## For Switch

**PWR SWITCH**




**LID SWITCH**

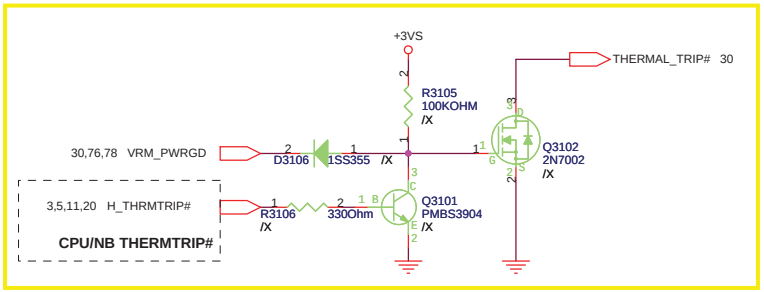


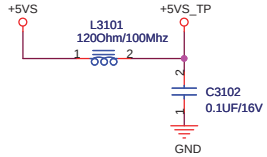

Note:
LID_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. Need to add bidirectional diode to protect this pin.

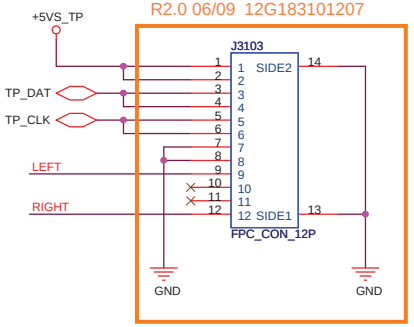
## For Thermal Control Method

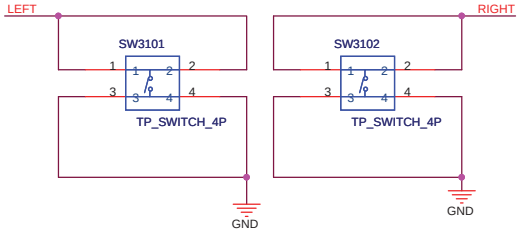
**11/20 Remove redundant components**

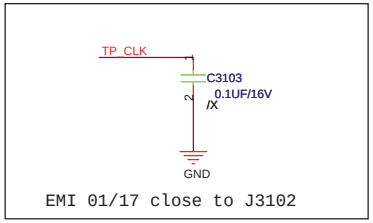


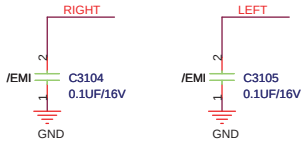

## Touchpad Connector



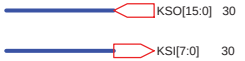



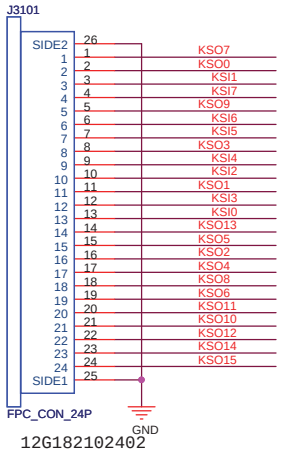




## Keyboard Connector

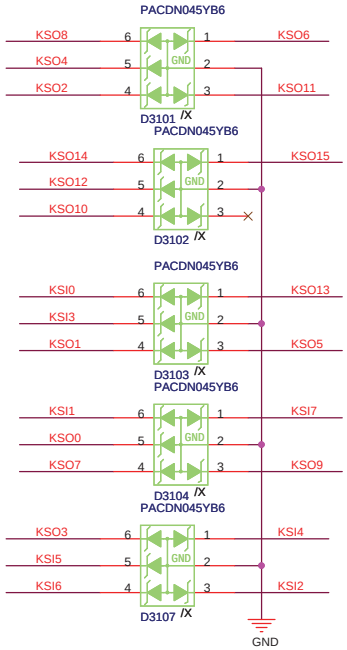


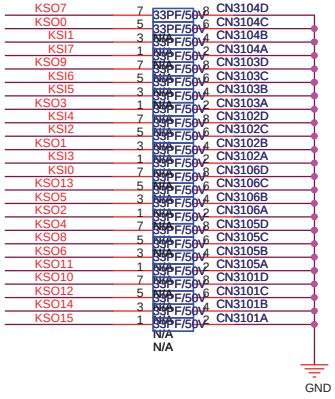

F7/N1 Keyboard




12G182102402

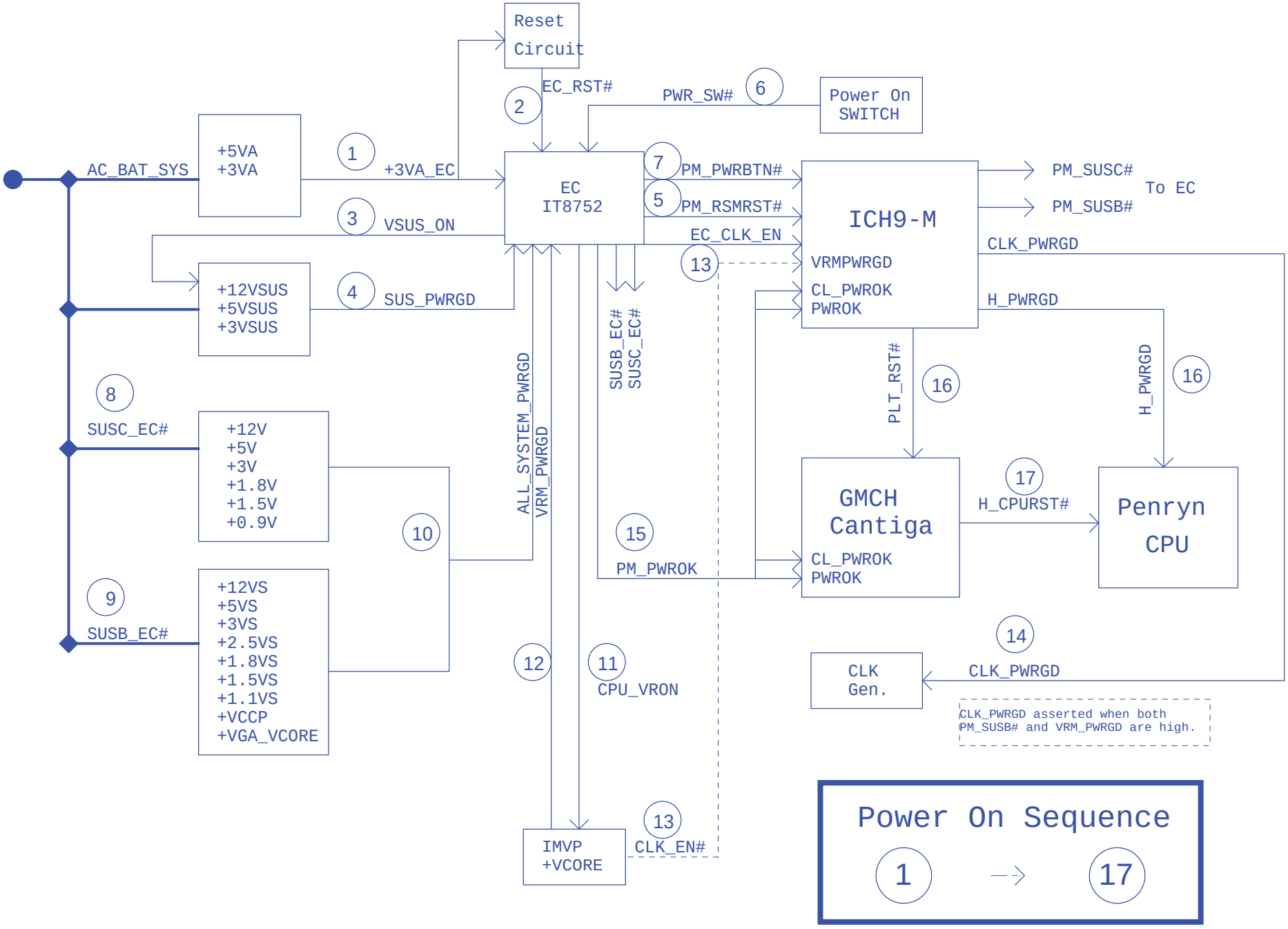
**11/02**



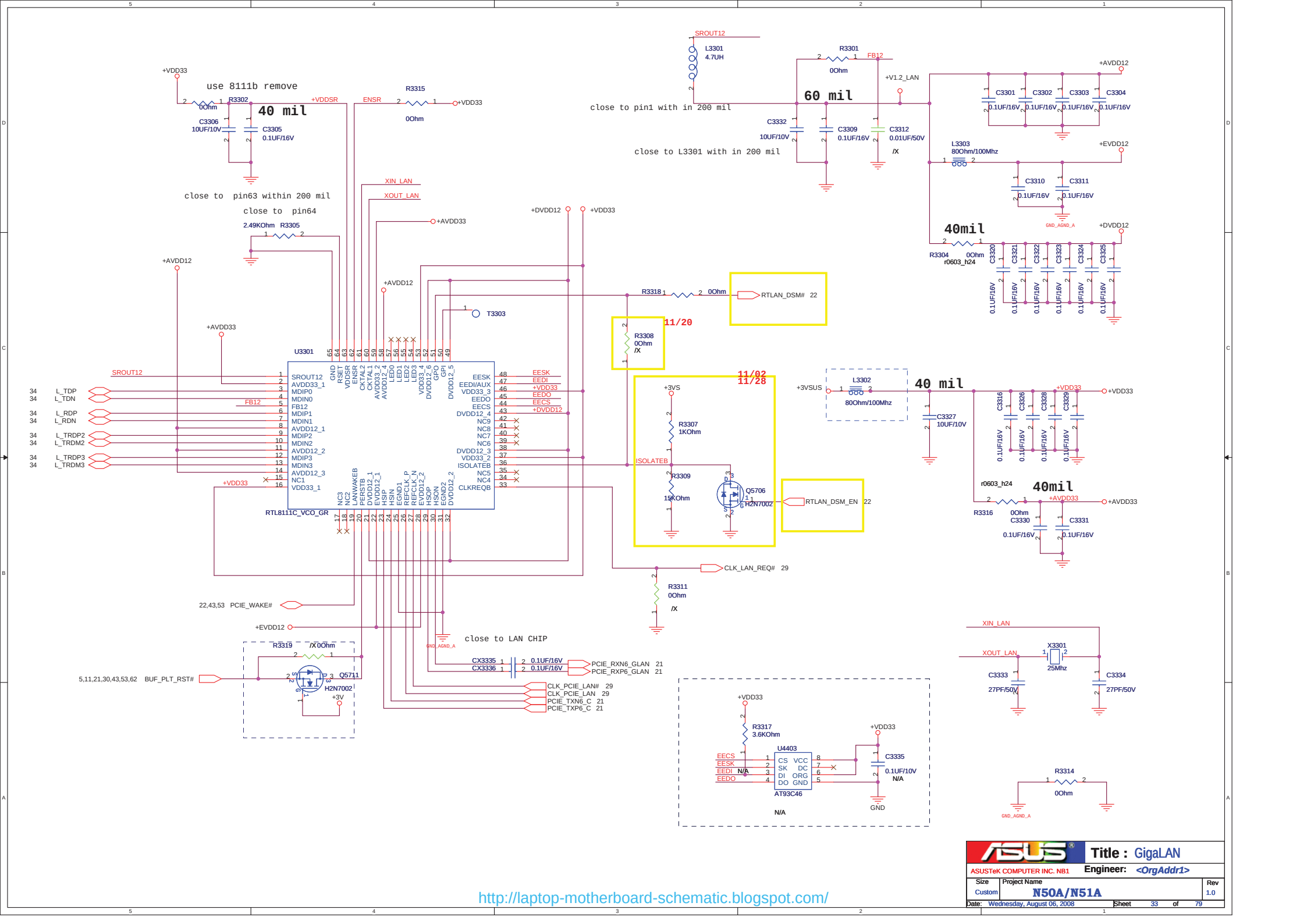

12G09103004P

| | | | |
|---|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | | Title : | EC_IT8511 (2/2) |
| | | Engineer: | <OrgAddr1> |
| Size: Custom | Project Name: N50A/N51A | | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 31 of 79 | | |



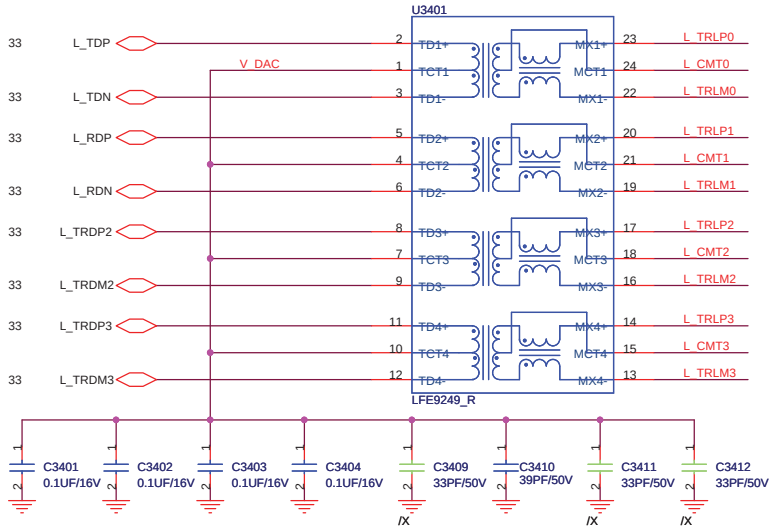


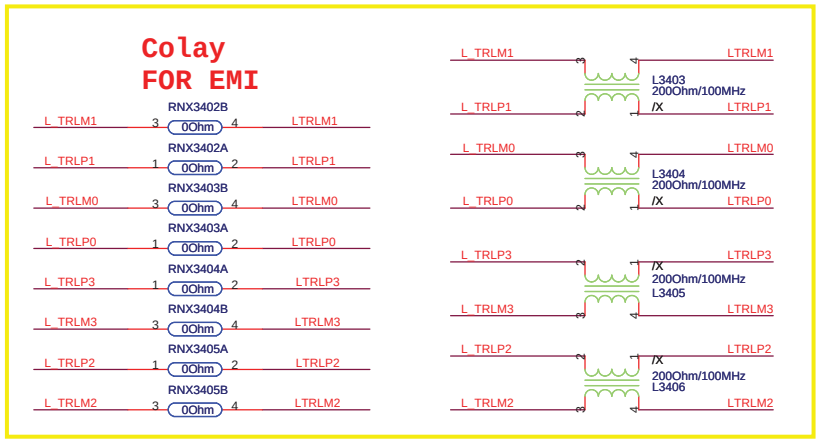

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : POWER-ON SEQUENCE | |
| | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Thursday, July 24, 2008 | Sheet 32 of 79 | |

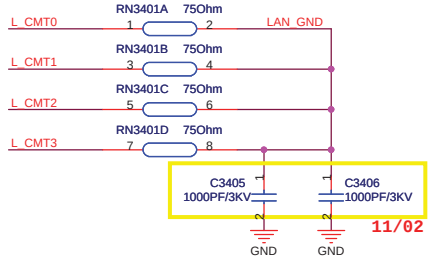


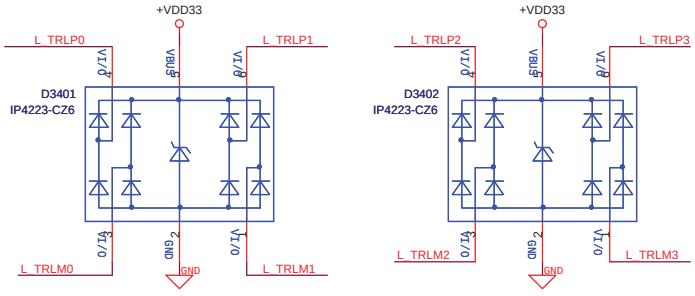


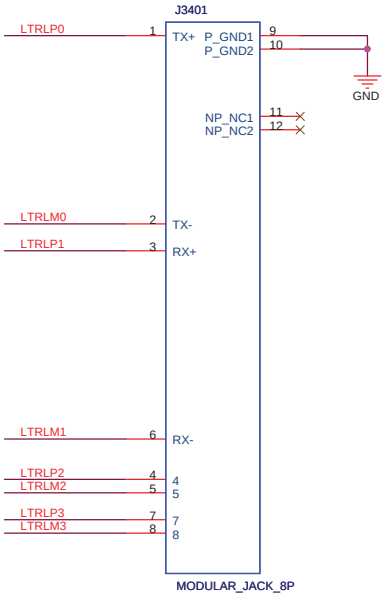

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : GigaLAN | |
| | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 33 of 79 | |



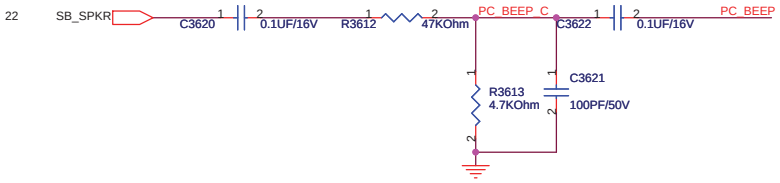

12G142111083



| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : RJ45 | |
| | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Friday, August 01, 2008 | Sheet 34 of 79 | |

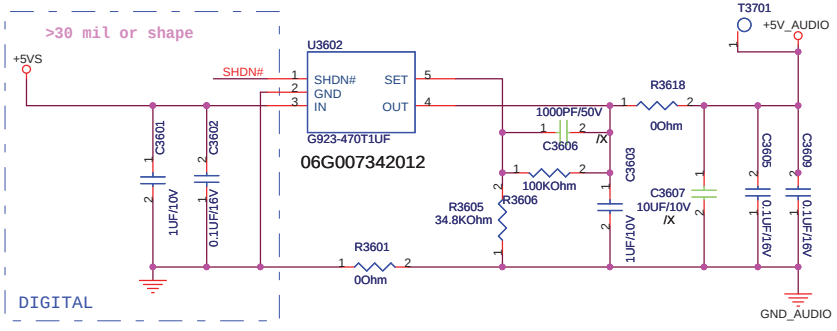
| | | | |
|---|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : MDC | | |
| | Engineer: <OrgAddr1> | | |
| Size: Custom | Project Name: N50A/N51A | | Rev: 1.0 |
| Date: Thursday, July 24, 2008 | Sheet 35 of 79 | | |

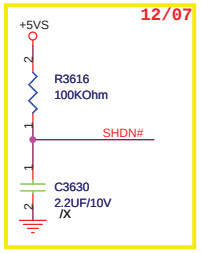
# PC BEEP

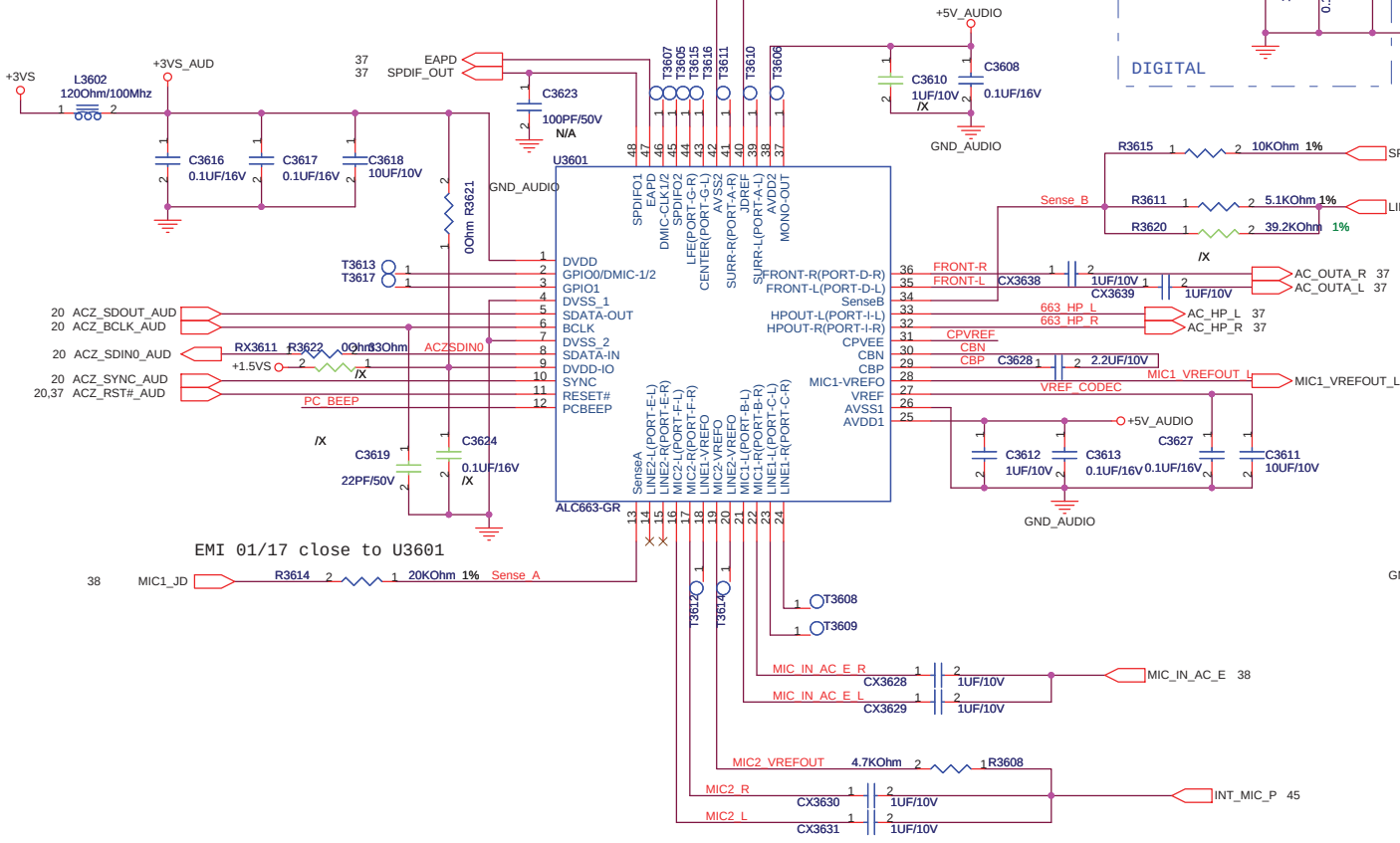



# Audio Power

**FOR ADJUST MODE:**
**Vo=1.25*(1+R3706/R3705)**
**= 1.25*( 1+ 100K/34.8K) = 4.84**



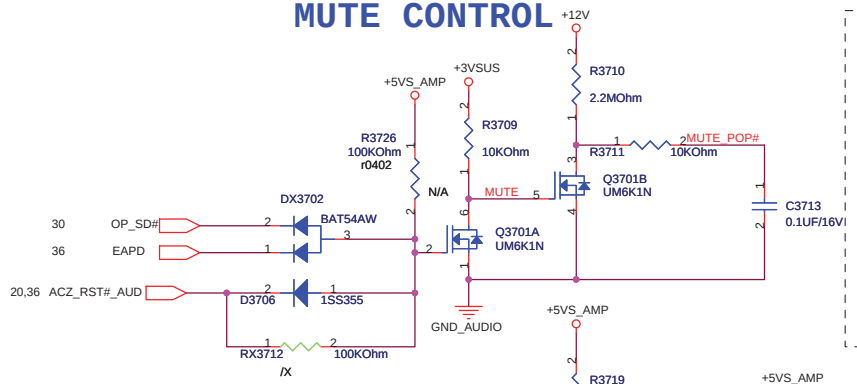

**Input impedence:64K ohm(Typical)**

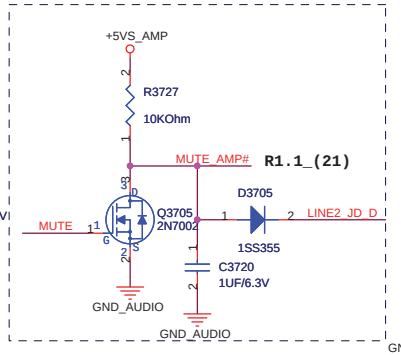
**12/07 ALC663 CHARGE PUMP**

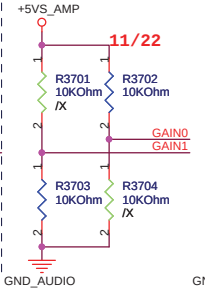


| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : CODEC ALC663 | |
| | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 36 of 79 | |

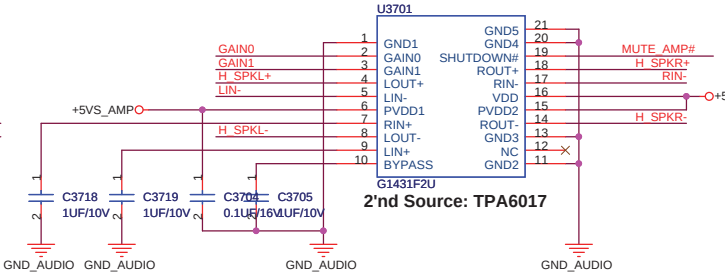
# MUTE CONTROL



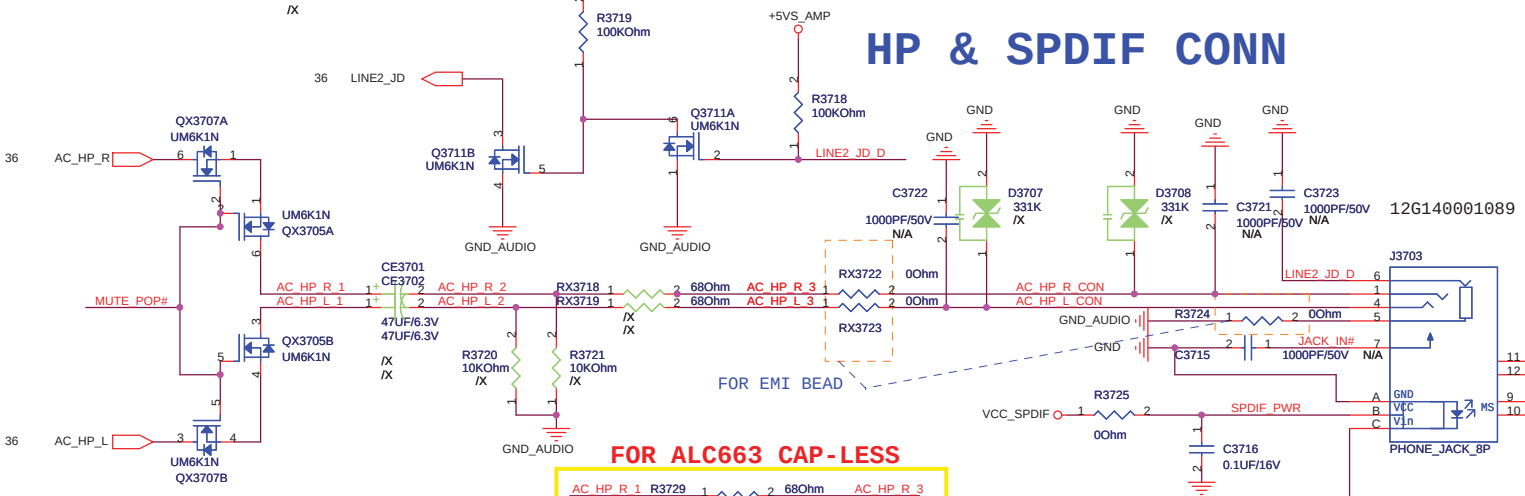




# SPEAKER AMP

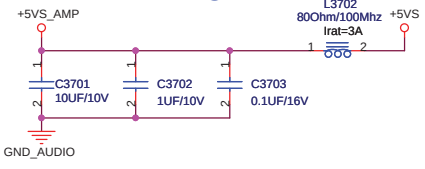



# HP & SPDIF CONN

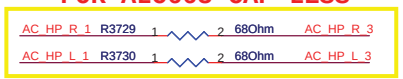


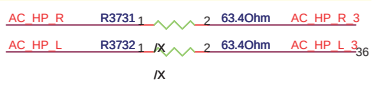

| GAIN0 | GAIN1 | Av(inv) |
|---|---|---|
| 0 | 0 | 6 dB |
| 0 | 1 | 10 dB |
| 1 | 0 | 15.6 dB |
| 1 | 1 | 21.6 dB |

# AMP POWER

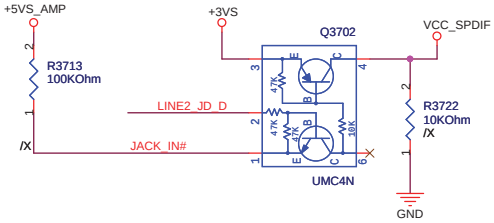



# FOR ALC663 CAP-LESS

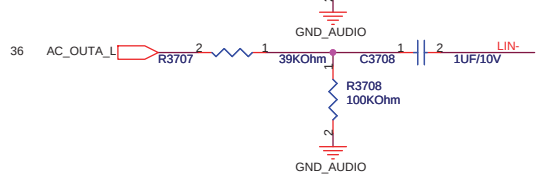


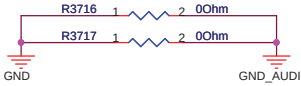


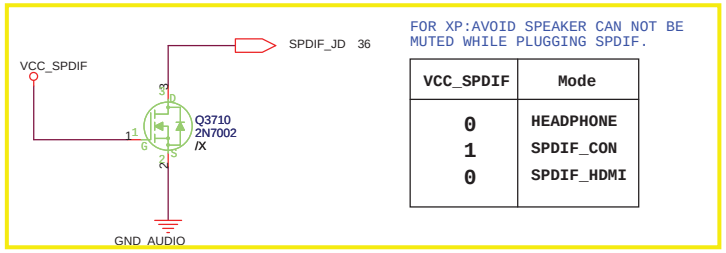



| JACK_IN# | LINE2_JD_D | Mode |
|---|---|---|
| 0 | 1 | SPDIF_CON |
| 0 | 0 | HEADPHONE,SPDIF_HDMI |
| 1 | 1 | SPDIF_HDMI |



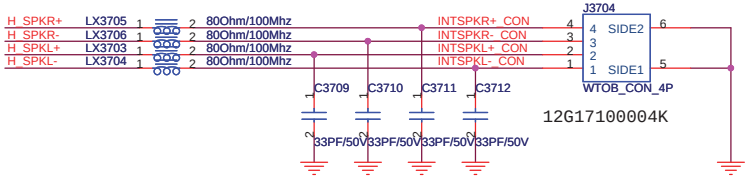

# JACK GND




| VCC_SPDIF | Mode |
|---|---|
| 0 | HEADPHONE |
| 1 | SPDIF_CON |
| 0 | SPDIF_HDMI |

# SPEAKER CONNECTOR(2W)






ASUSTeK COMPUTER INC. NB1

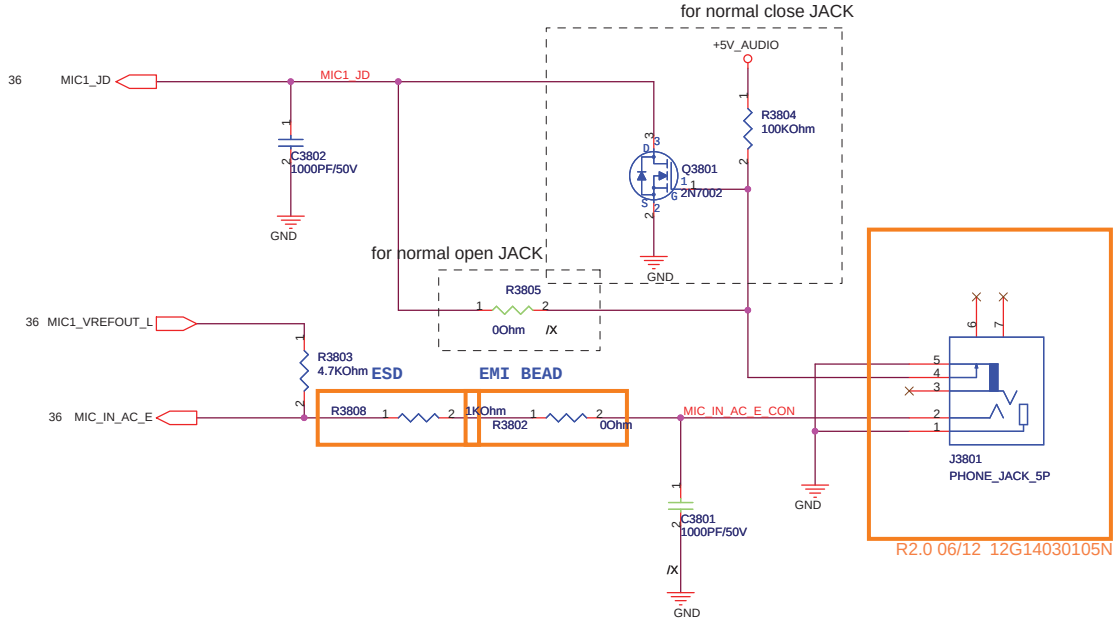
Title : AUDIO AMP

Engineer: <OrgAddr1>

| Size | Project Name | Rev |
|---|---|---|
| Custom | N50A/N51A | 1.0 |

Date: Wednesday, August 06, 2008 Sheet 37 of 79

# EXTERNAL MICROPHONE






| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : MIC&LINEIN | |
| | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Friday, August 01, 2008 | Sheet 38 of 79 | |

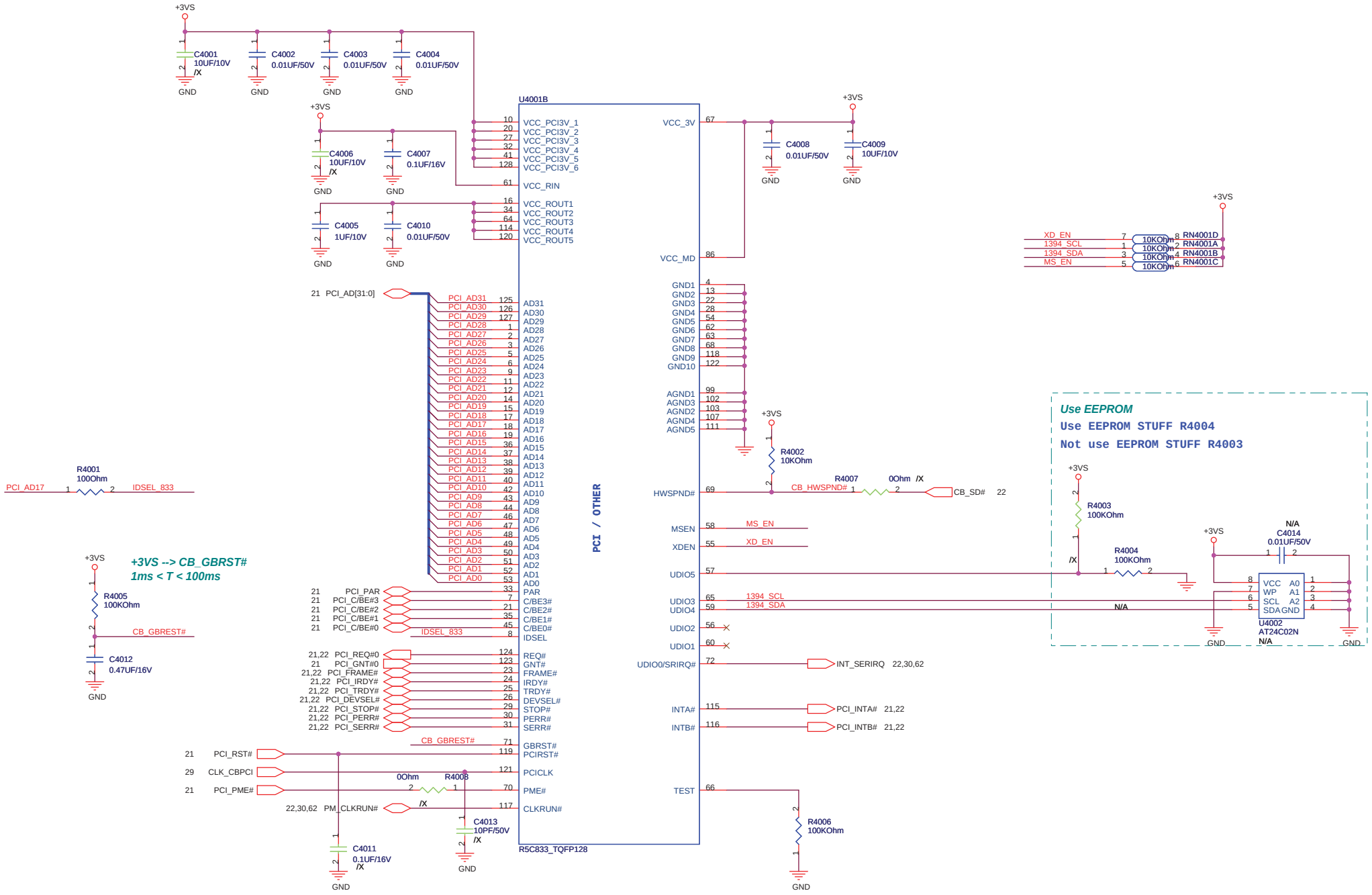
Title : DSP

ASUSTeK COMPUTER INC. NB1

Engineer: <OrgAddr1>

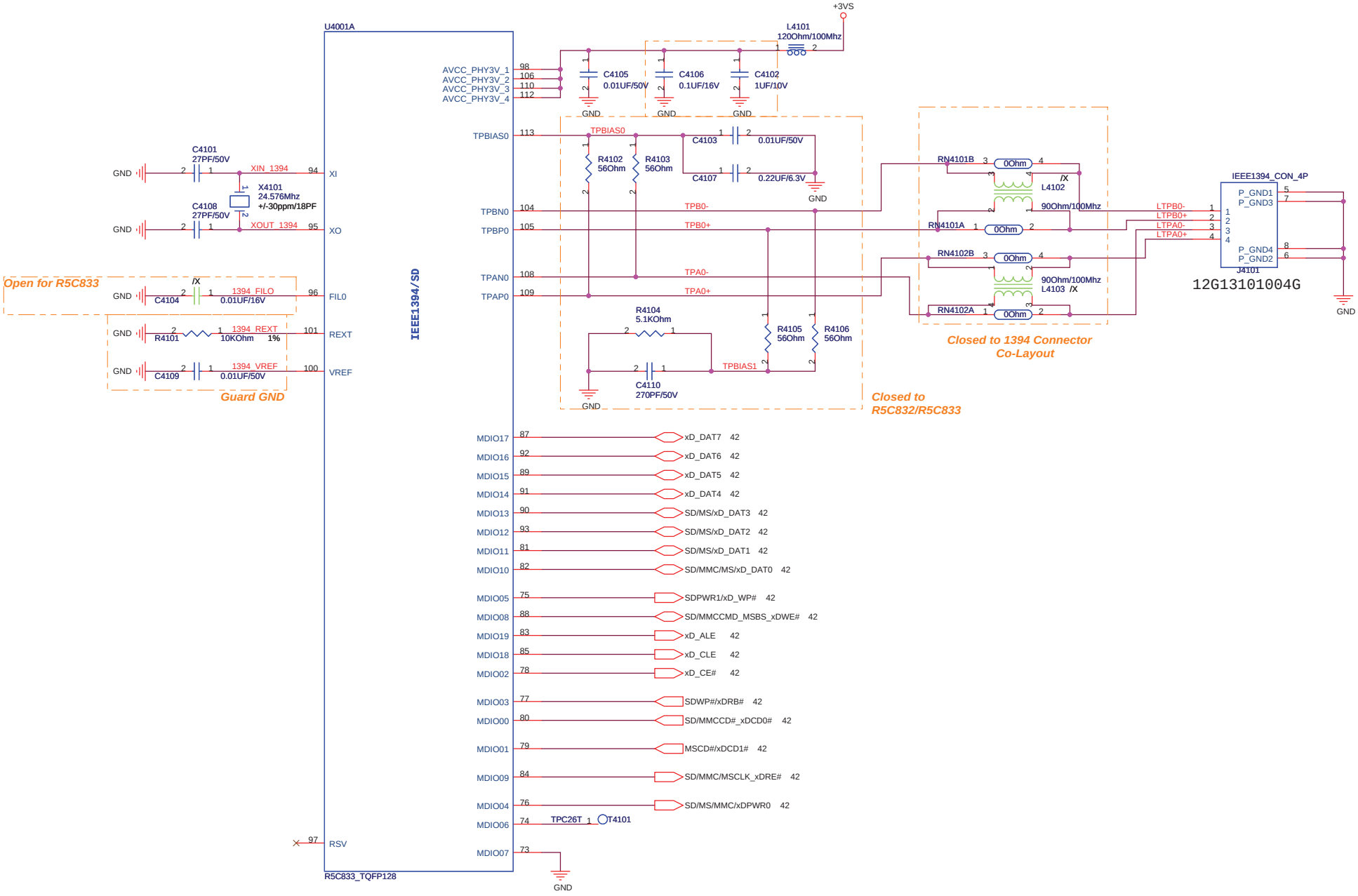
| Size | Project Name | Rev |
|---|---|---|
| A | N50A/N51A | 1.0 |

Date: Thursday, July 24, 2008 Sheet 39 of 79



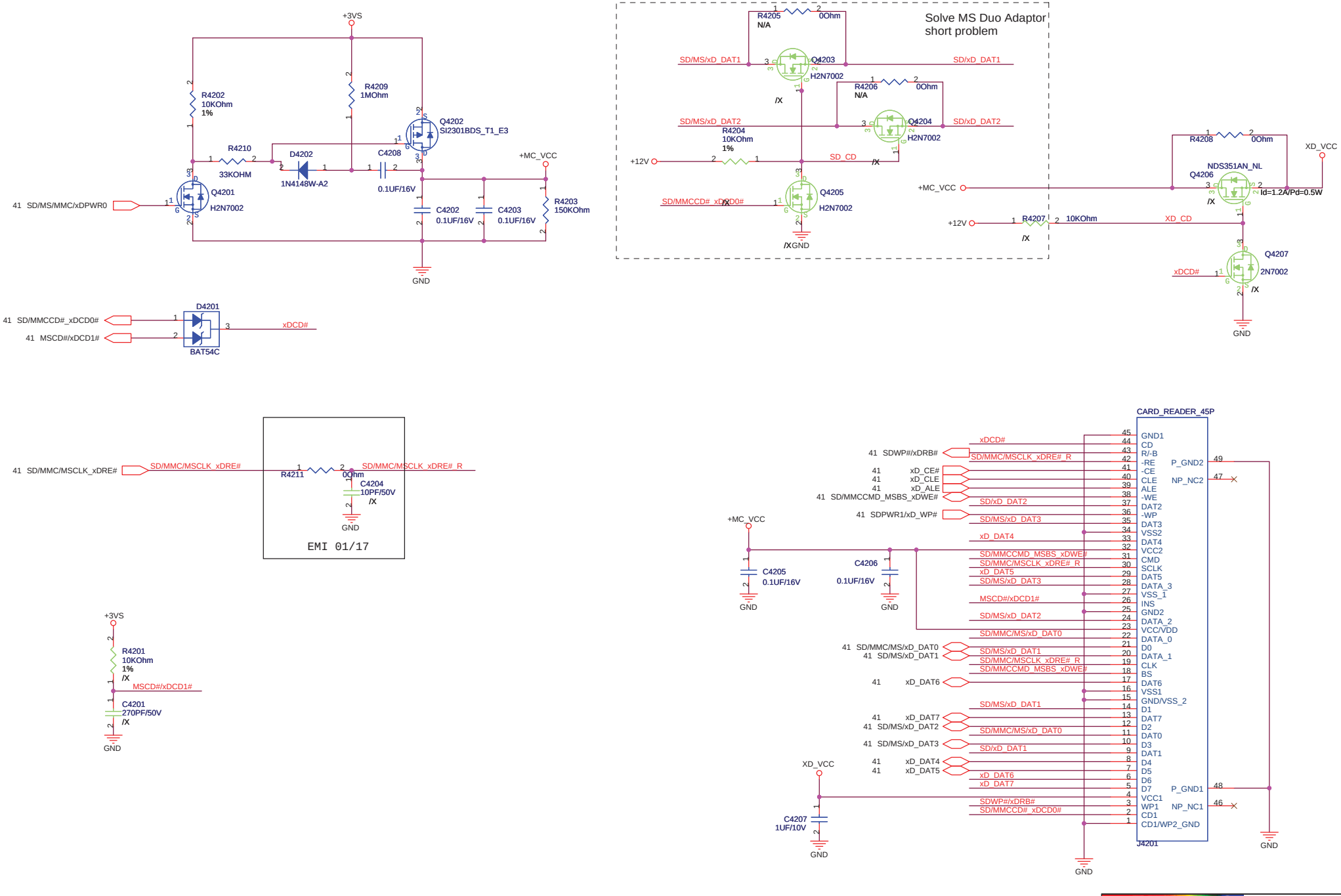



| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : CARDBUS R5C833 (1) | |
| | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Tuesday, August 12, 2008 | Sheet 40 of 79 | |

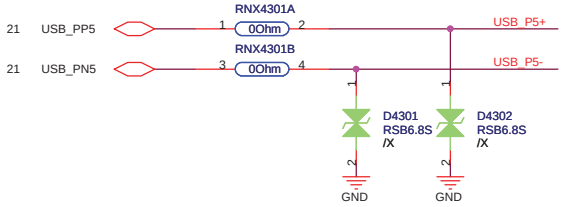




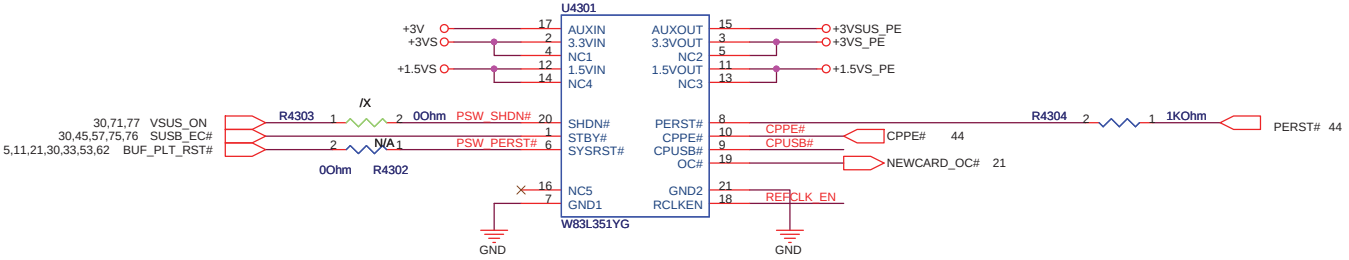

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : CARDBUS R5C833 (2) | |
| | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Thursday, August 07, 2008 | Sheet 41 of 79 | |




| | | | |
|---|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : 1394&CardReader CON | | |
| | Engineer: <Enginner Name> | | |
| Size: Custom | Project Name: N50A/N51A | | Rev: 1.0 |
| Date: Monday, August 11, 2008 | Sheet 42 of 79 | | |

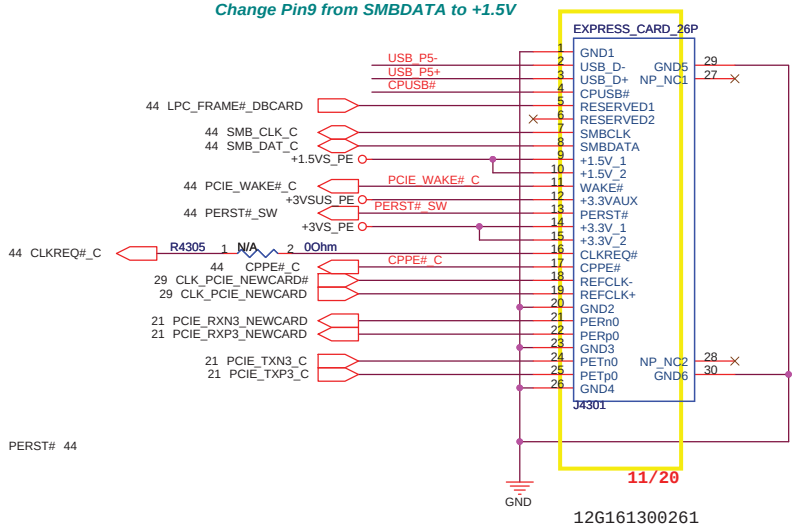



1st source:06G030091010



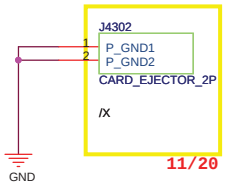

!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

NewCard Header

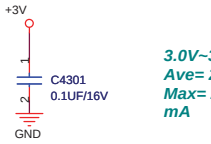



12G161300261

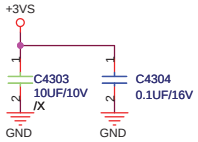
NewCard Ejecter

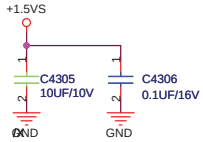



12G21C102604

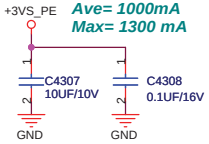



3.0V~3.6V
Ave= 200mA
Max= 275 mA

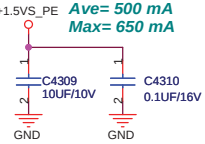



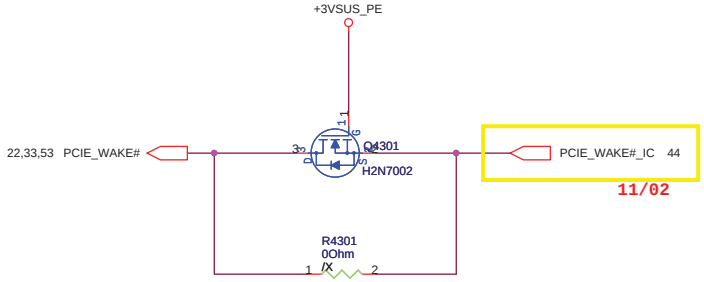



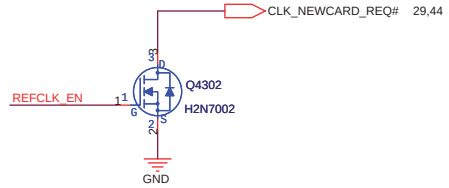

3.0V~3.6V
Ave= 1000mA
Max= 1300 mA




1.35V~1.65V
Ave= 500 mA
Max= 650 mA



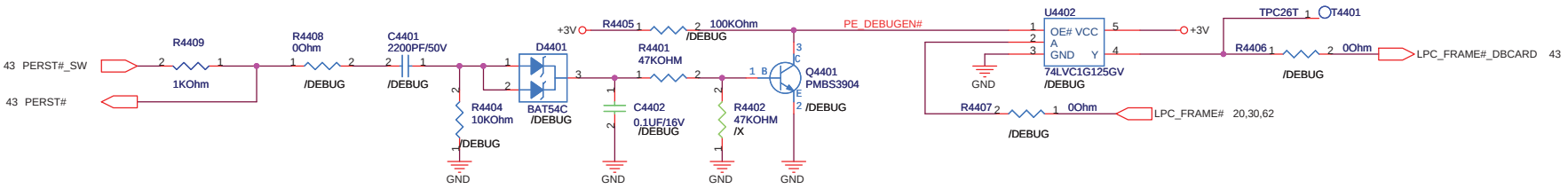



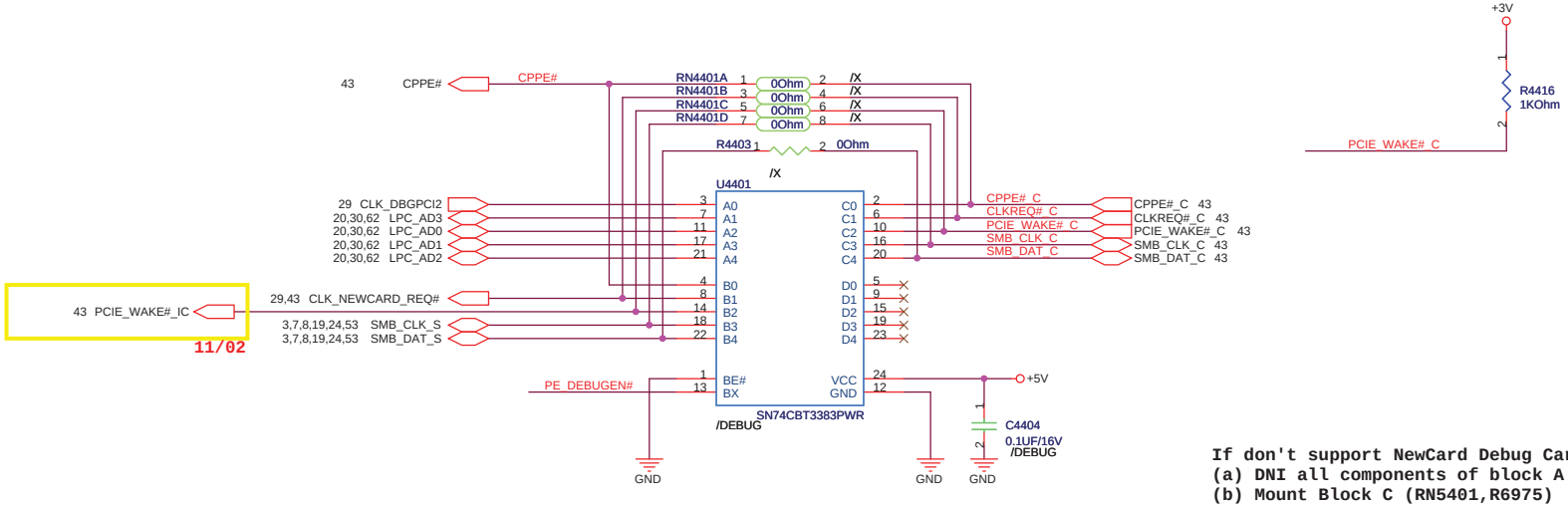






| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : NEW CARD | |
| | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 43 of 79 | |

# Block A



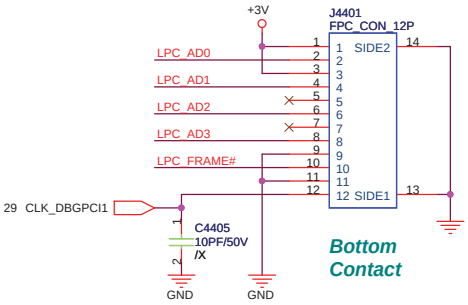


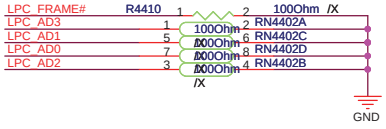


If don't support NewCard Debug Card,Pls do
(a) DNI all components of block A
(b) Mount Block C (RN5401,R6975)

## *For PCMCIA Debug Card*

**If support NewCard Debug Card,**
**Pls don't mount all components.**



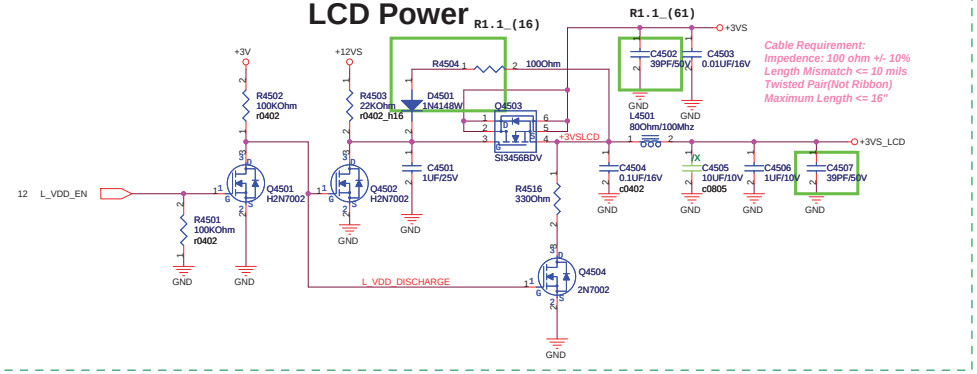





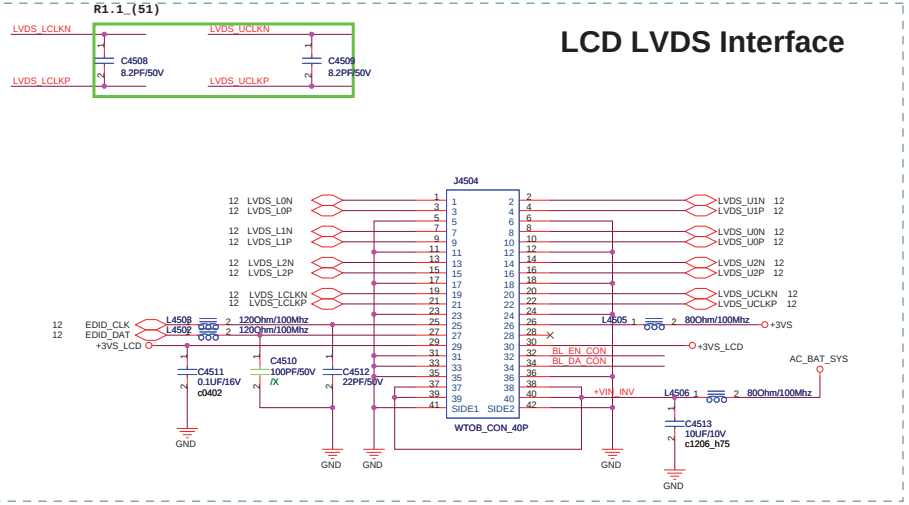

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : DEBUG | |
| | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Monday, August 04, 2008 | Sheet 44 of 79 | |

## LCD Backlight Control

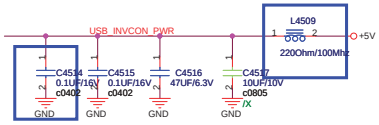
### LCD Power

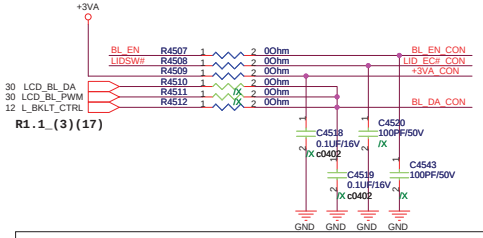


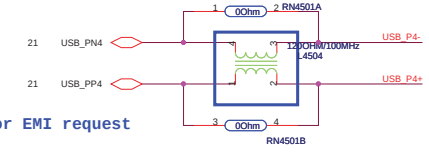

## LCD LVDS Interface



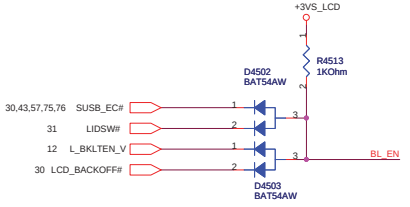

*Inverter Interface/Speaker CONN.*

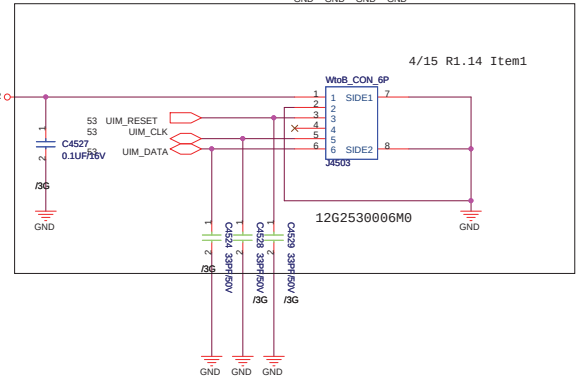


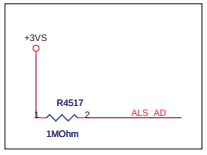



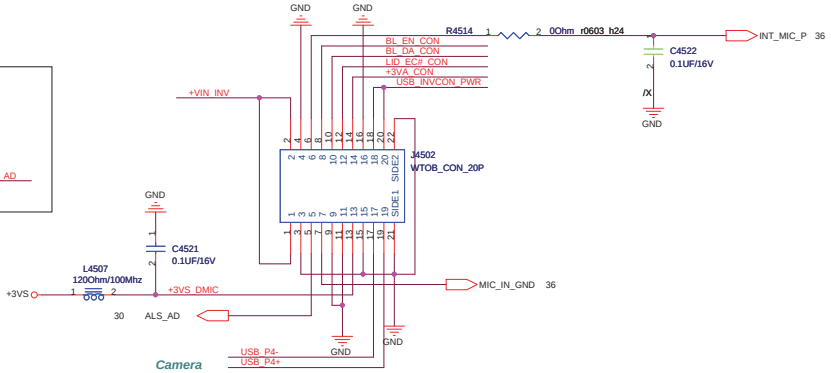



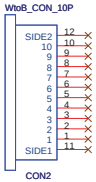

R1.1_(59) change for EMI request



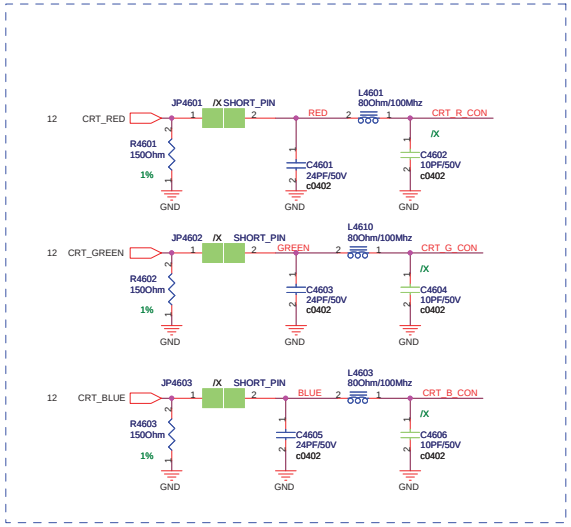



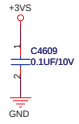



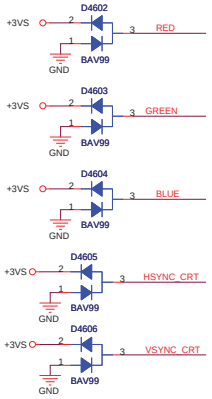




| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : LVDS | |
| | Engineer: <OrgAddr1> | |
| Size: C | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Monday, August 11, 2008 | Sheet 45 of 79 | |

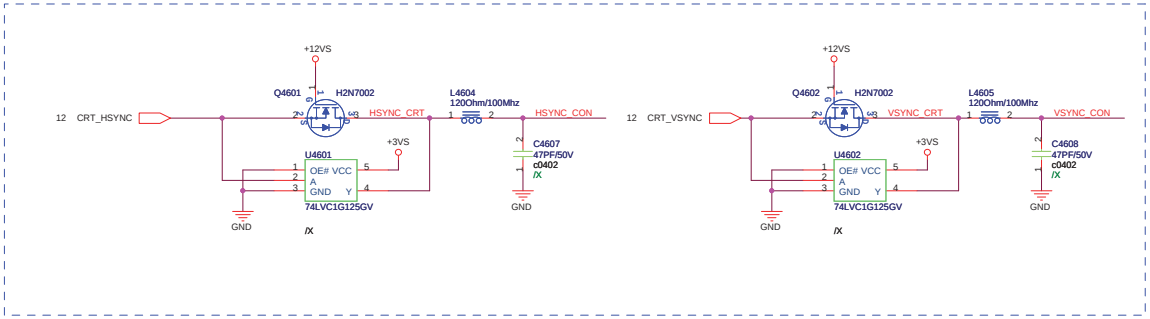


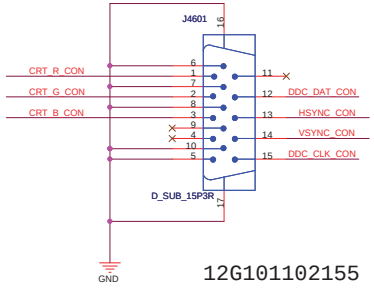




Place a 0.1uF CAP across the ESD Diode close

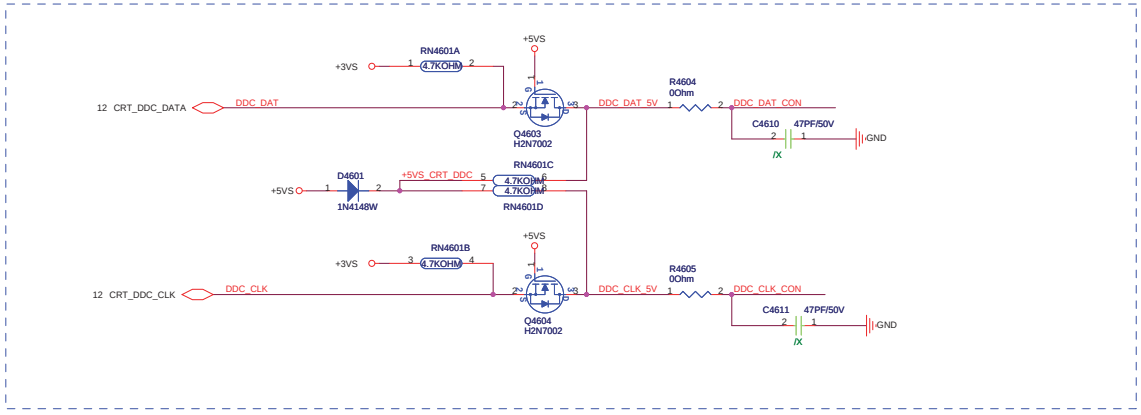



**PLACE ESD Diodes near VGA port**



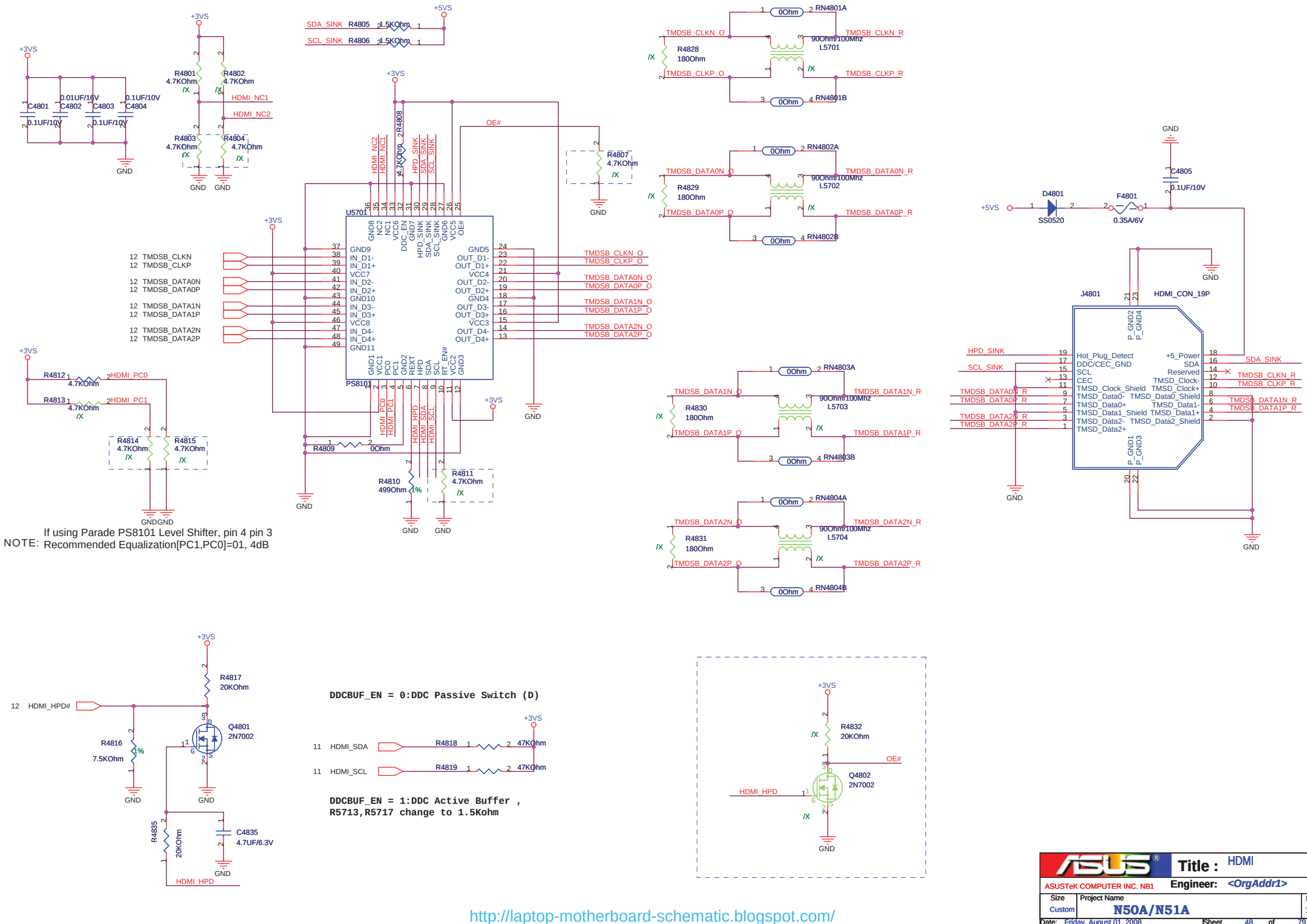

12G101102155






| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : CRT | |
| | Engineer: <OrgAddr1> | |
| Size: C | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 46 of 79 | |

| | |
|---|---|
| Title : DVI | |
| ASUSTeK COMPUTER INC. NB1 | Engineer: <OrgAddr1> |
| Size: A | Project Name: N50A/N51A |
| Rev: 1.0 | |
| Date: Thursday, July 24, 2008 | Sheet 47 of 79 |

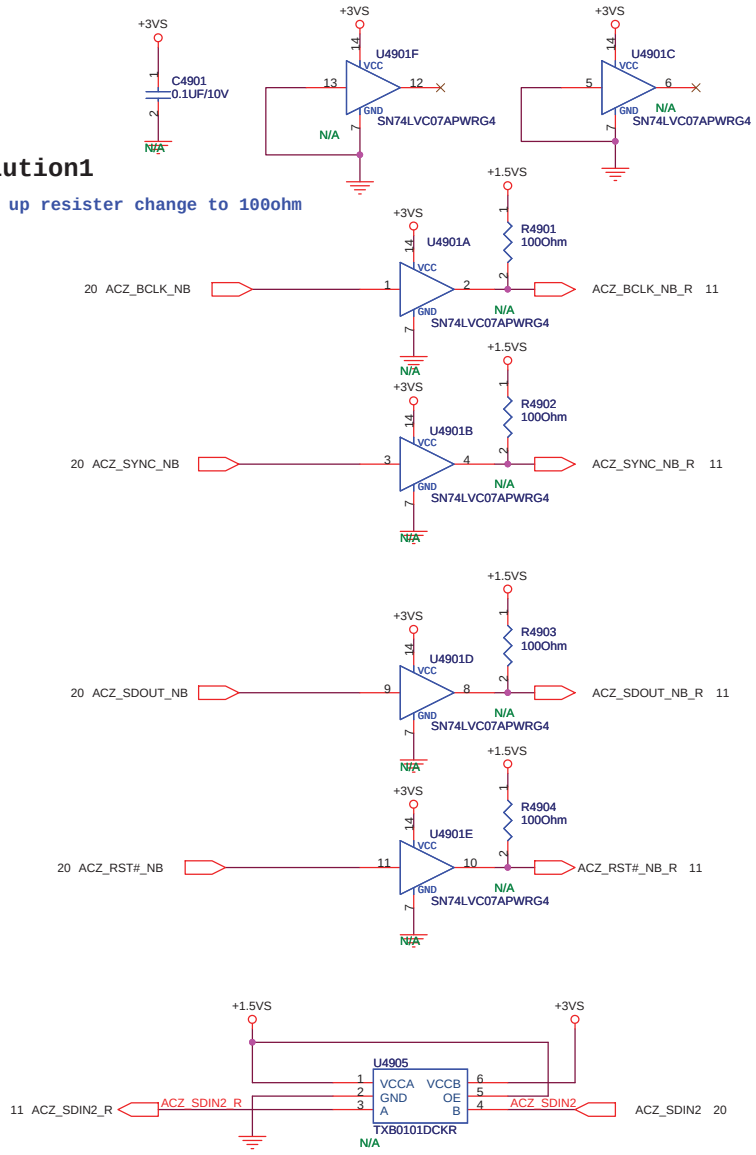





| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : HDMI | |
| | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Friday, August 01, 2008 | Sheet 48 of 79 | |

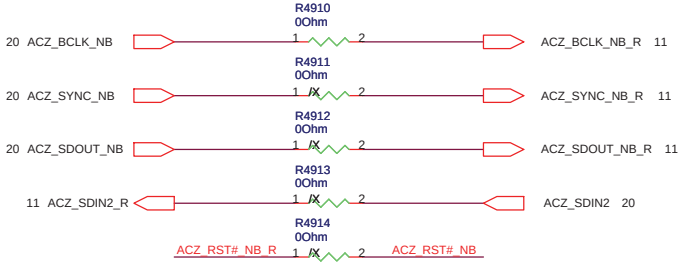
## Solution1

pull up resister change to 100ohm




## Solution2

for 1.5V HDA




/X

ASUSTeK COMPUTER INC. NB1

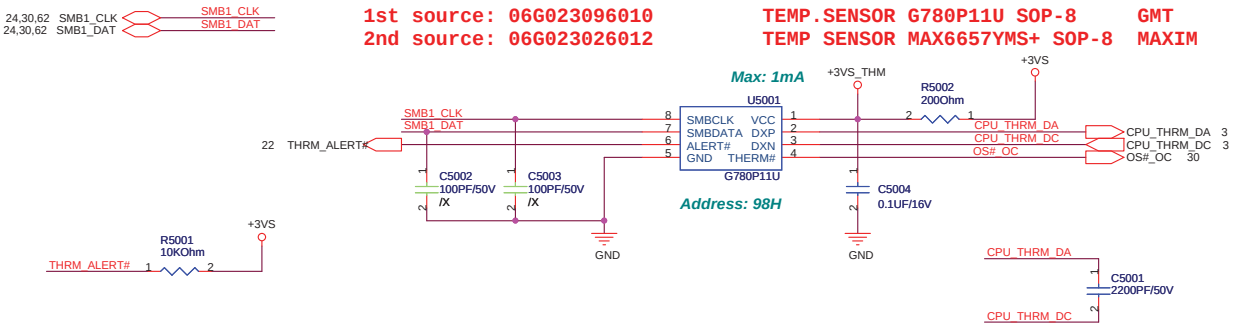
Title :

Engineer: <OrgAddr1>

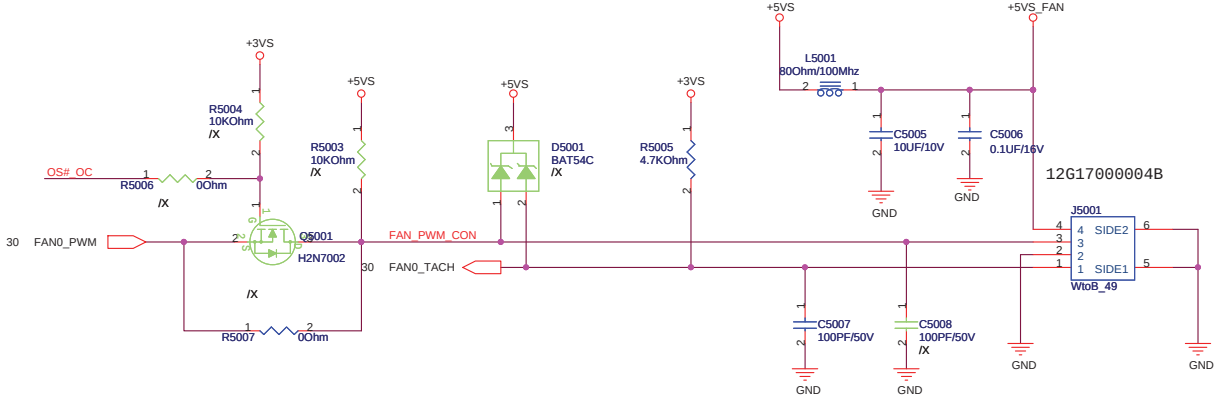
| Size | Project Name | Rev |
|---|---|---|
| Custom | N50A/N51A | 1.0 |

Date: Friday, August 01, 2008 Sheet 49 of 79

## Thermal Sensor



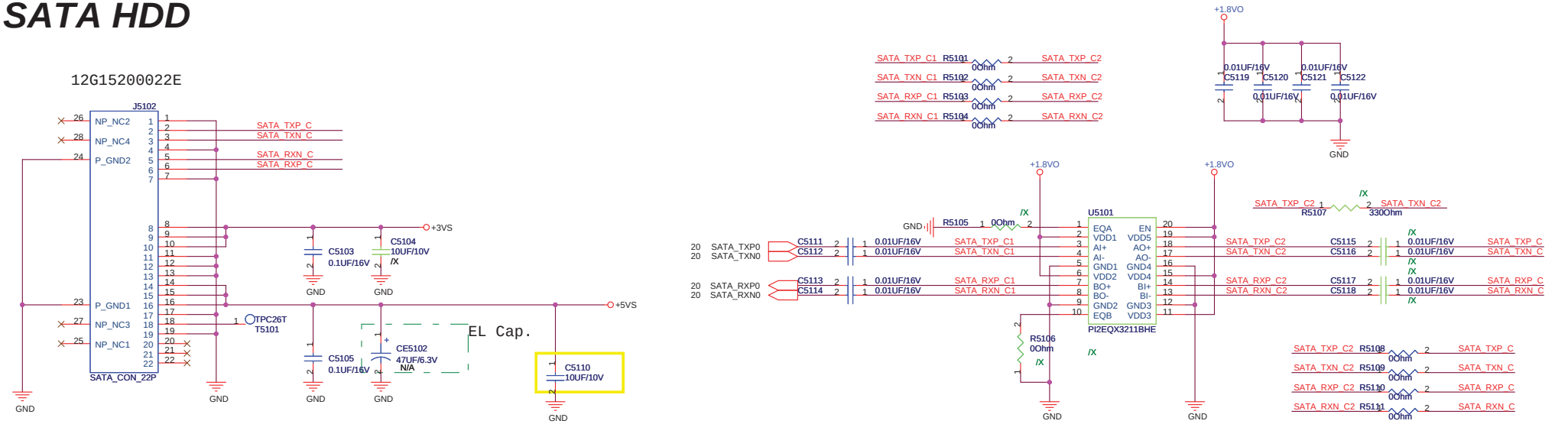

## DC FAN Control



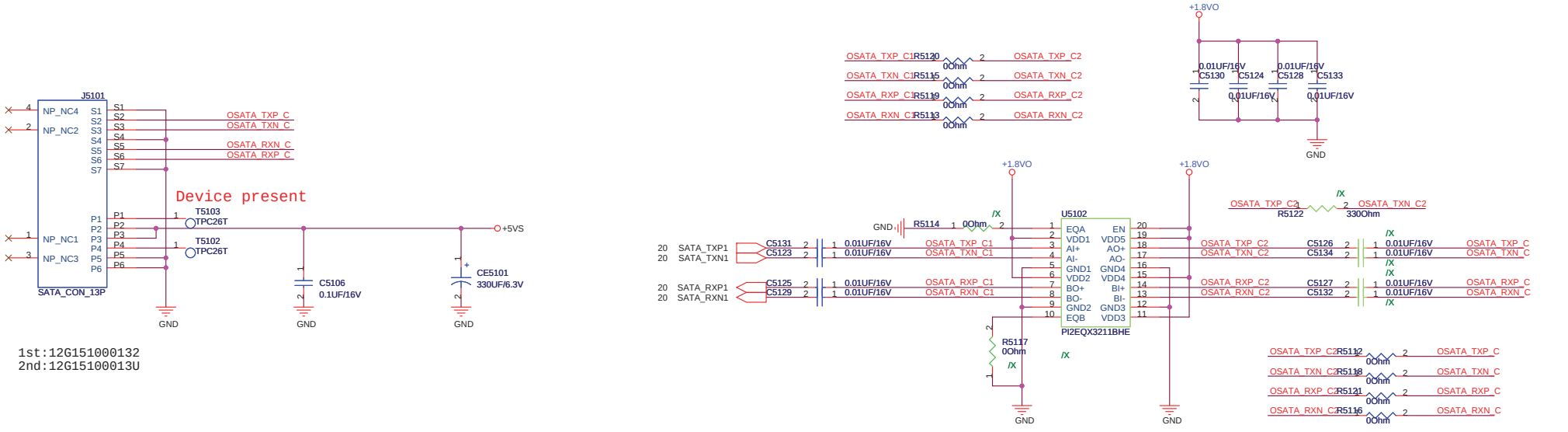



| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : Thermal & Fan | |
| | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 50 of 79 | |

# SATA HDD

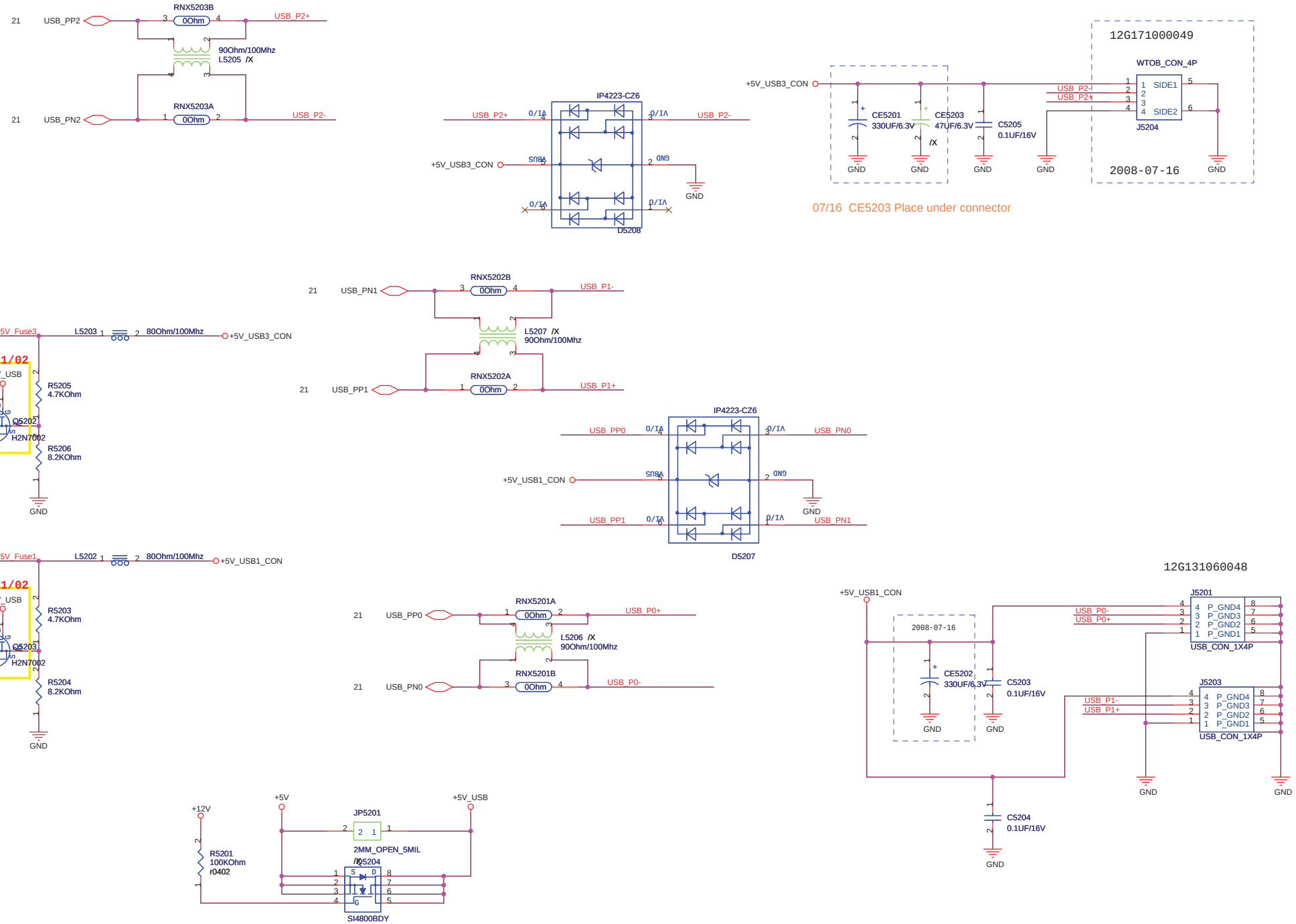



# ODD



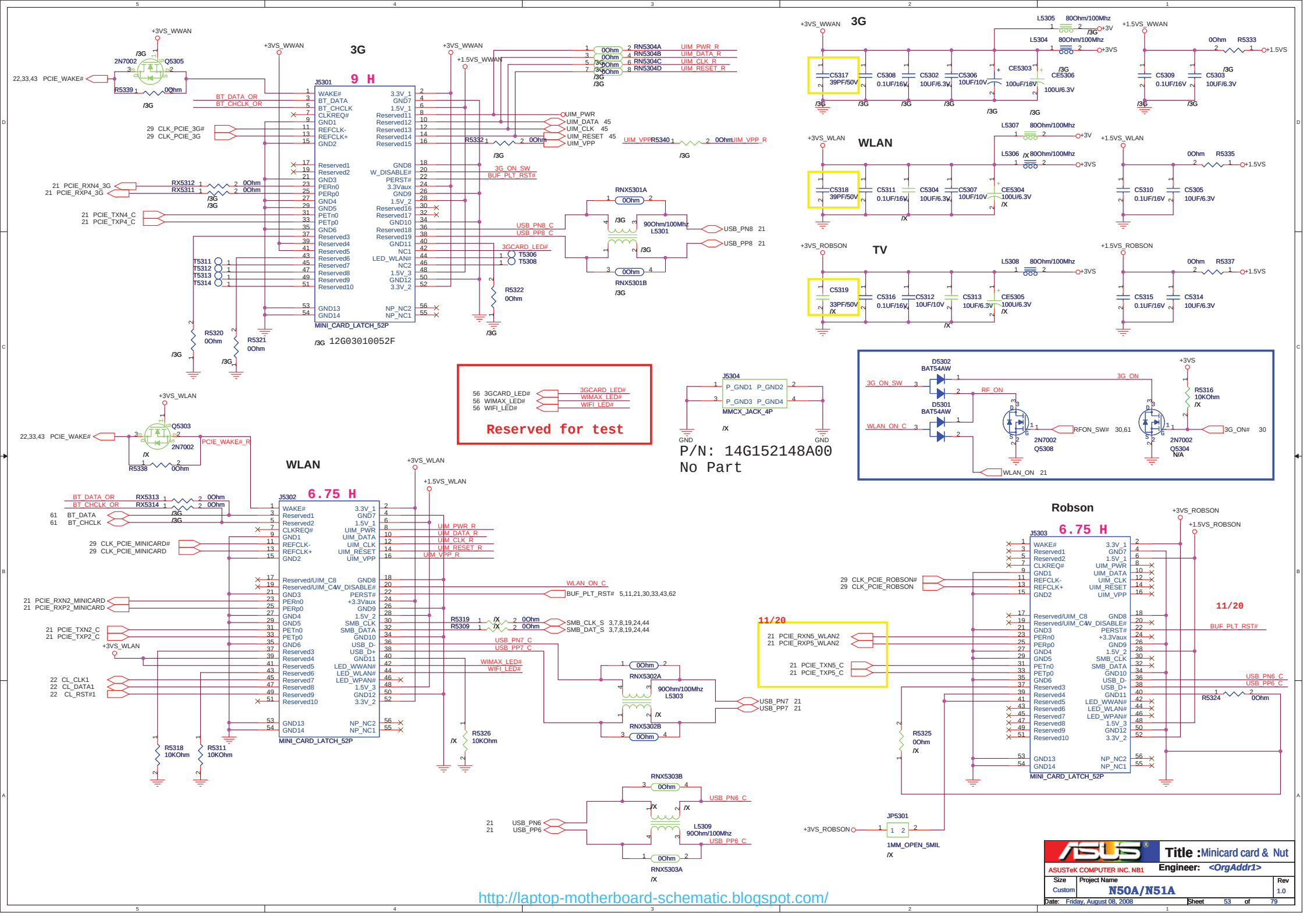



| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : HDD & CD-ROM | |
| | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 51 of 79 | |





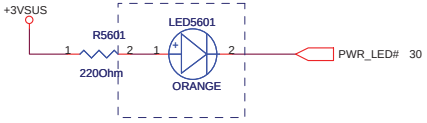

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : USB CONN X 3 | |
| | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 52 of 79 | |


3G
9 H
J5301
MINI_CARD_LATCH_52P
12G03010052F
WLAN
6.75 H
J5302
MINI_CARD_LATCH_52P
Reserved for test
P/N: 14G152148A00
No Part
Robson
6.75 H
J5303
MINI_CARD_LATCH_52P
11/20
TV
WLAN
3G
http://laptop-motherboard-schematic.blogspot.com/
ASUSTeK COMPUTER INC. NB1
Title :Minicard card & Nut
Engineer: <OrgAddr1>
Project Name
N50A/N51A
Rev
1.0
Date: Friday, August 08, 2008
Sheet 53 of 79

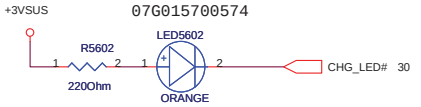
| | |
|---|---|
| Title : | Port Docking |
| ASUSTeK COMPUTER INC. NB1 | Engineer: *<OrgAddr1>* |
| Size: A | Project Name: **N50A/N51A** |
| Rev: 1.0 | |
| Date: Thursday, July 24, 2008 | Sheet 54 of 79 |

| | |
|---|---|
| Title : | Super I/O & FIR |
| ASUSTeK COMPUTER INC. NB1 | Engineer: <OrgAddr1> |
| Size: A | Project Name: N50A/N51A |
| Rev: 1.0 | |
| Date: Thursday, July 24, 2008 | Sheet 55 of 79 |

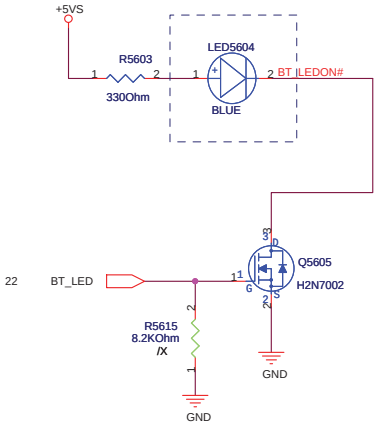
## For Power LED



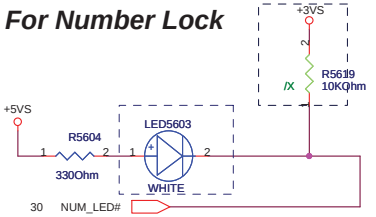

## For Battery LED



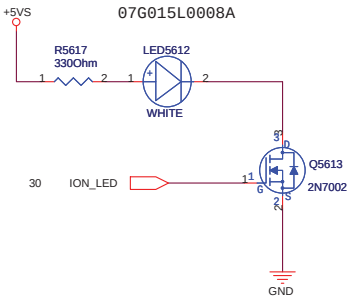

## For BT LED



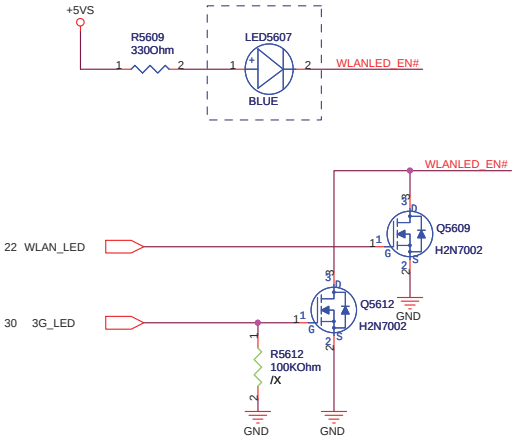

## For Number Lock



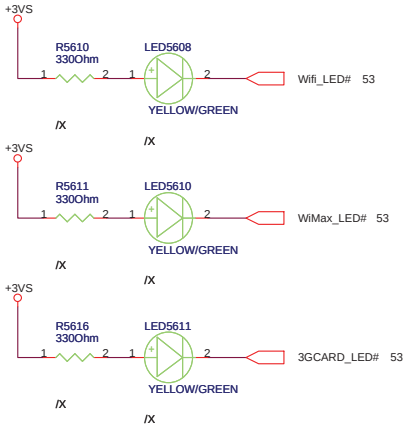

## For Ionizer



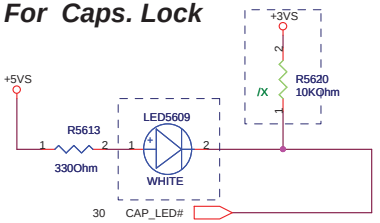

## For WireLess LED



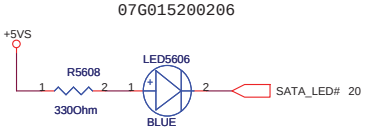

## LEDs for testing

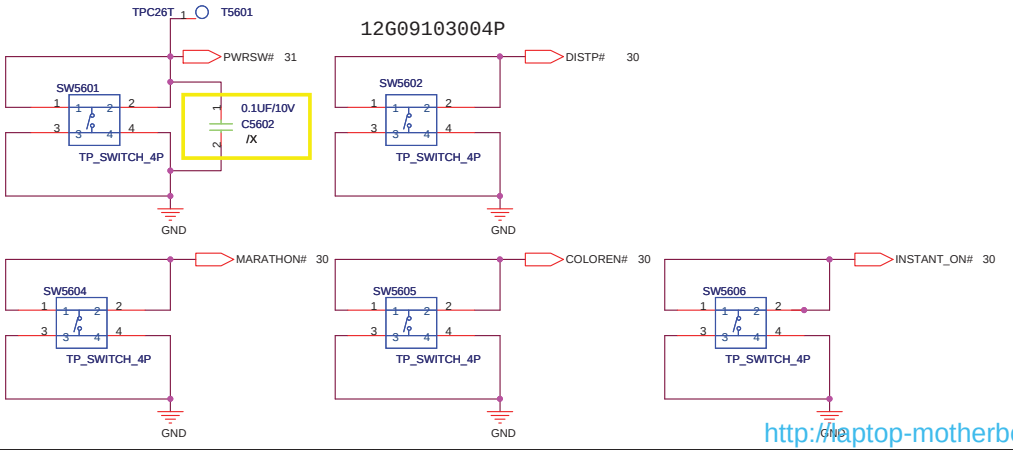



## For Caps. Lock

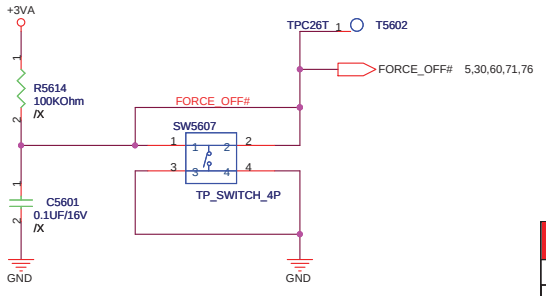



## For SATA/IDE LED



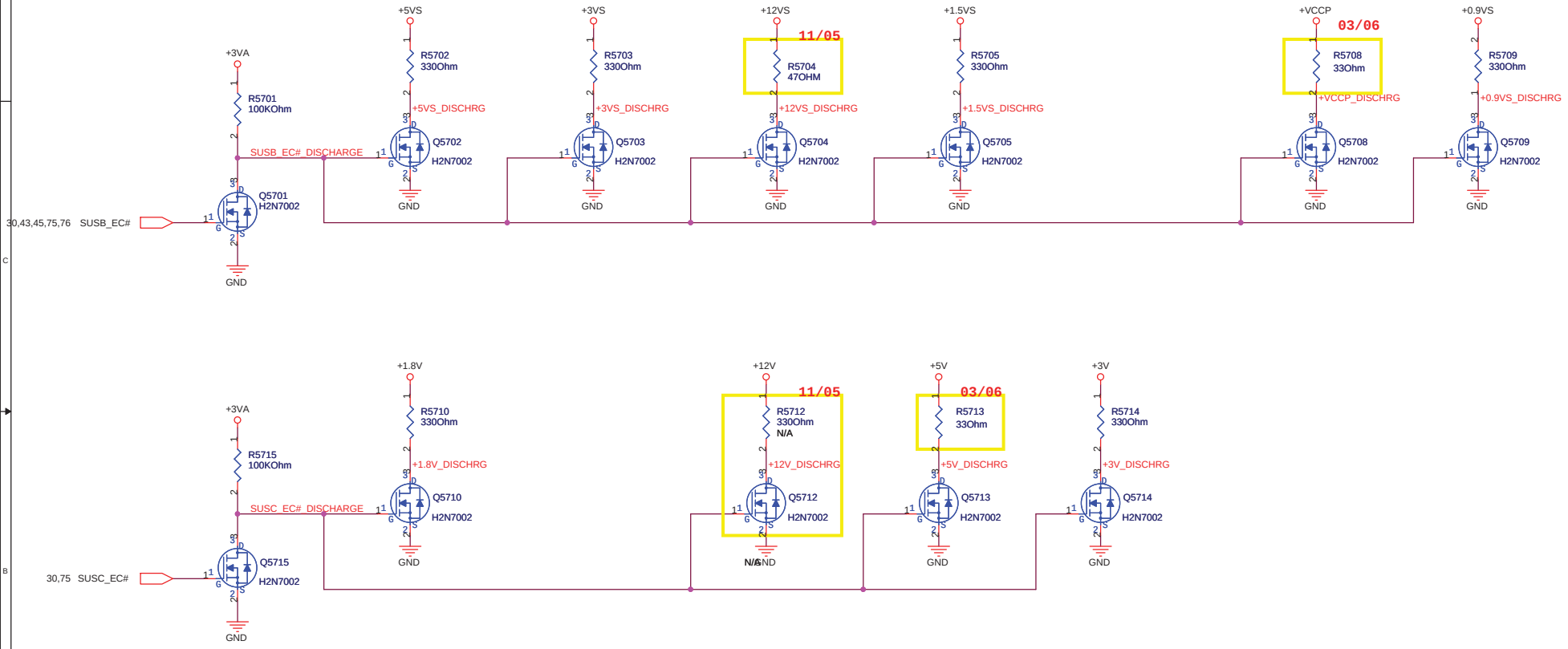




## SHUT_DOWN#






| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : LED/TP/SW | |
| | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 56 of 79 | |






| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : DISCHARGE | |
| | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 57 of 79 | |

Title : UWB Minicard card

ASUSTeK COMPUTER INC. NB1

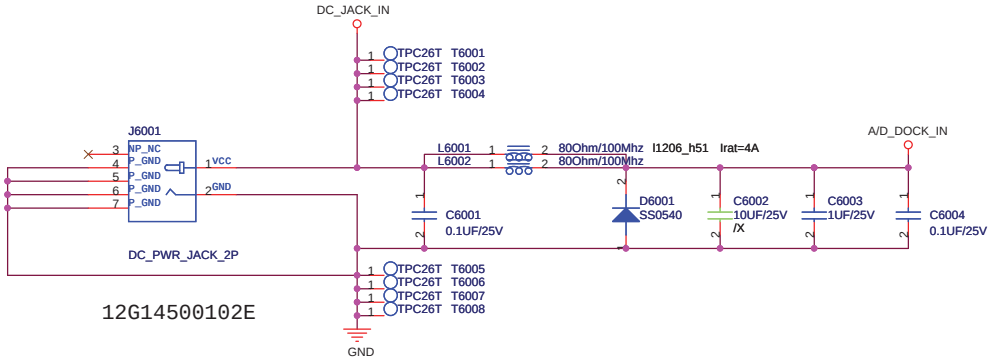
Engineer: <OrgAddr1>

| Size | Project Name | Rev |
|---|---|---|
| Custom | N50A/N51A | 1.0 |

Date: Wednesday, August 06, 2008 Sheet 58 of 79

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : | |
| | Engineer: <OrgAddr1> | |
| Size: A | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Thursday, July 24, 2008 | Sheet 59 of 79 | |

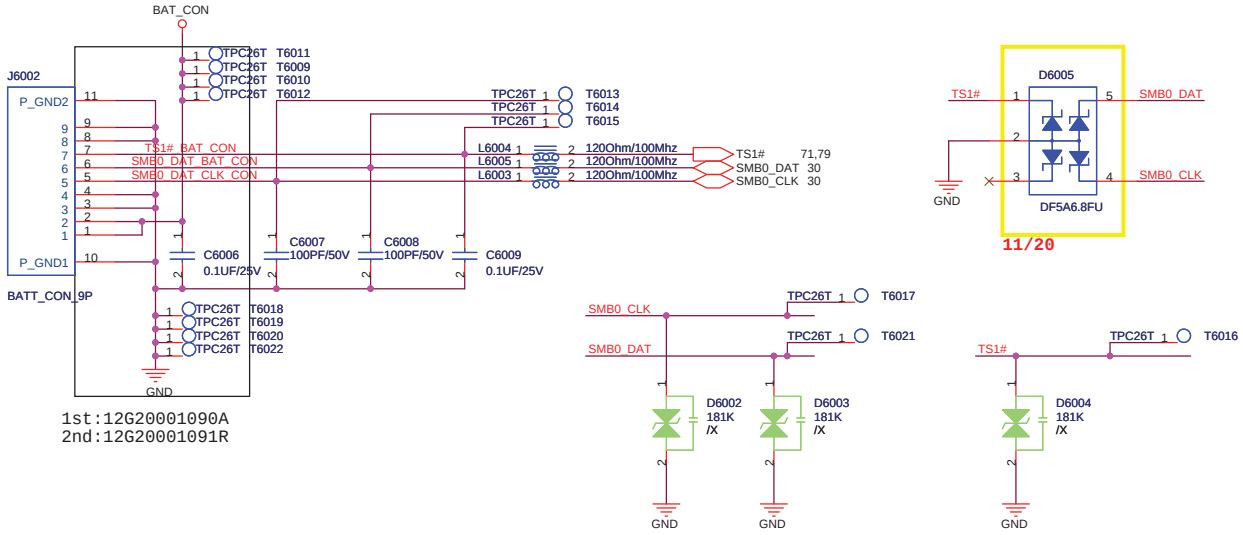
# DC IN




12G14500102E

# BAT IN

3/11 Pin define follow Battery protection board



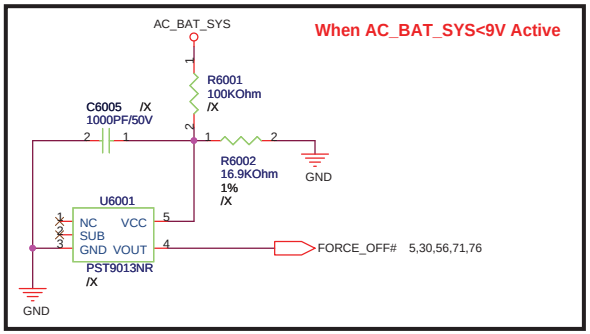

1st:12G20001090A
2nd:12G20001091R




11/20



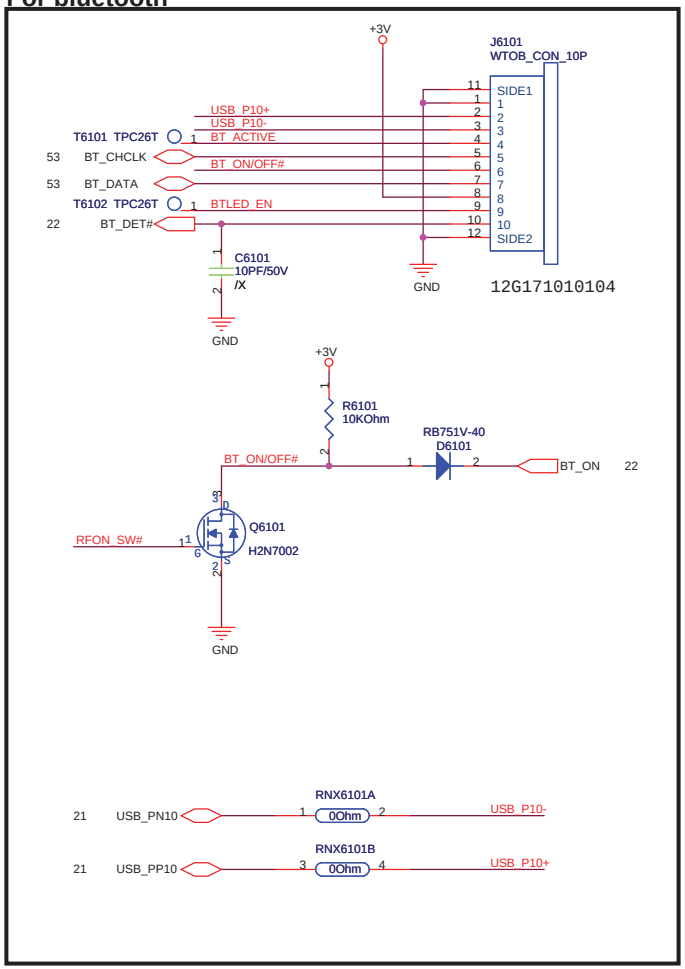

## Without Battery & Pull out Adapter





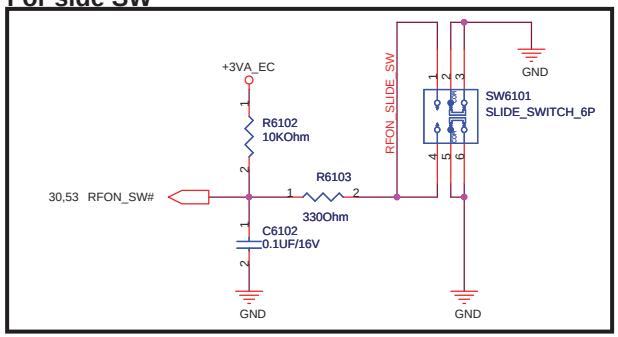

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : DC Jack & Battery CONN | |
| | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 60 of 79 | |

## For bluetooth




## For side SW

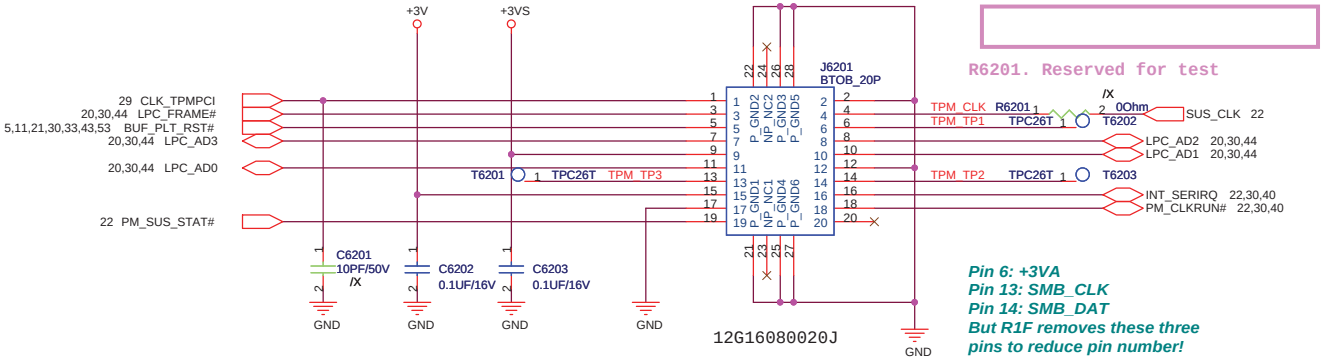
12G090070063






| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : BlueTooth | |
| | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 61 of 79 | |

## For TPM module

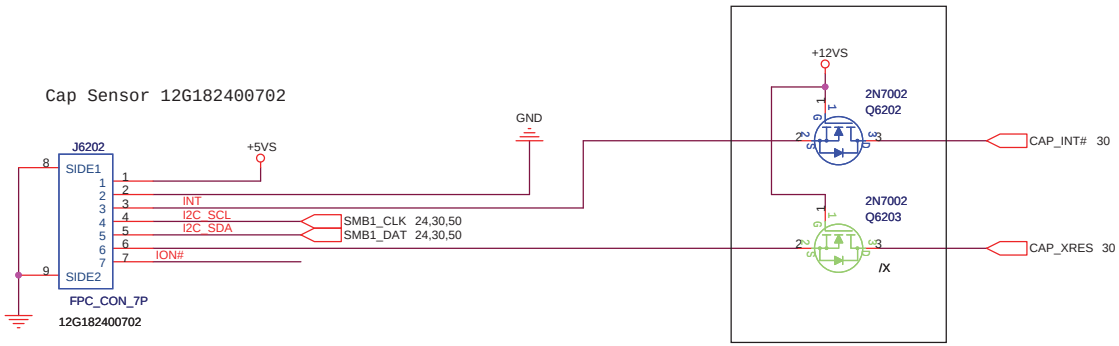



R6201. Reserved for test

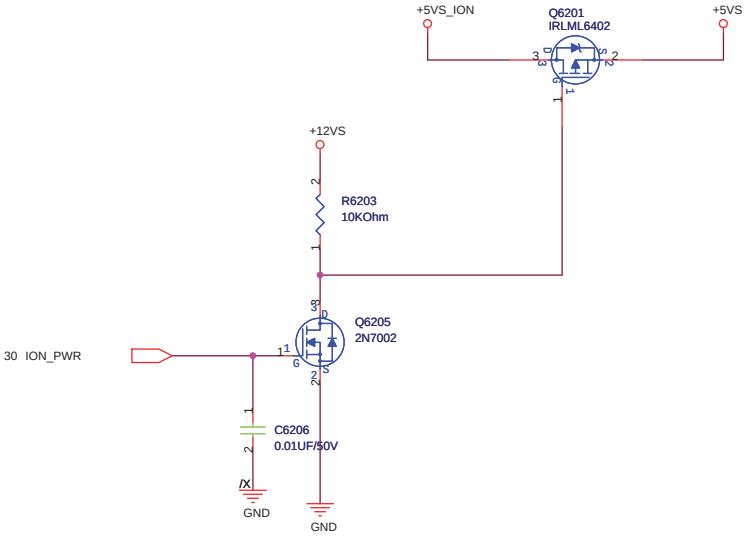
*Pin 6: +3VA*
*Pin 13: SMB_CLK*
*Pin 14: SMB_DAT*
*But R1F removes these three pins to reduce pin number!*

R1.10 04/08 Item1 level shift

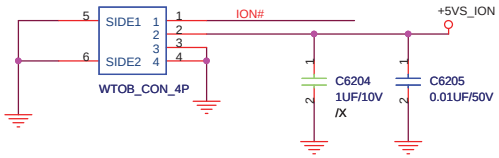
Cap Sensor 12G182400702




R1.10 04/08 Item2 Ion Power control schematic

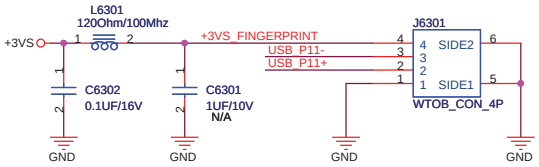


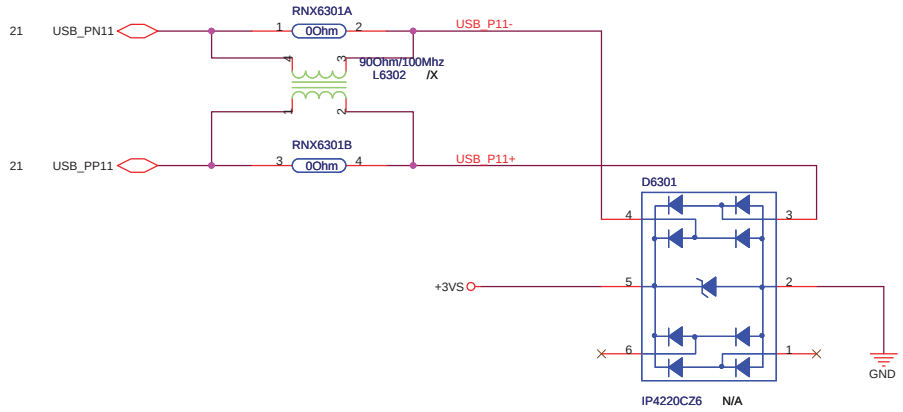

ION 12G17100004K






| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : TPM | |
| | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 62 of 79 | |






| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : Fingerprint | |
| | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 63 of 79 | |

Title : TUN

ASUSTeK COMPUTER INC. NB1

Engineer: <OrgAddr1>

| Size | Project Name | Rev |
|---|---|---|
| B | N50A/N51A | 1.0 |

Date: Thursday, July 24, 2008 Sheet 64 of 79

R1.11 04/10 EMI

U6501 EMI_SPRING_PAD
U6502 EMI_SPRING_PAD
U6503 EMI_SPRING_PAD
/EMI
GND

R2.0 06/18 reserve for EMI

H6524 H6525 H6526 S335D91N /X GND

固定孔
H6527 C79D79N /X

FOR SCREW HOLE

H6501 H6502 H6503 H6505 H6506 H6507 H6509 H6510 H6512 H6513 H6514 H6518 H6523 H6528 H6511 S335D91N CR226X236D91N /X GND

FOR TPM (BOT) 13GN7510M270 FOR MDC (TOP)

H6201 L4E_1A GND

FOR CPU

H6516 H6520 H6521 H6522 CT268B158D138 /X GND

13G021029050
FOR 3G (BOT)
H5301 A40M20-64AS
H5302 A40M20-64AS
GND

FOR ROBSON (BOT)
H5303 H5304 CT217B67D47 GND

FOR WLAN (BOT)

13G021043050
FOR UWB (BOT)
H5801 H5802 CT217B67D47 GND

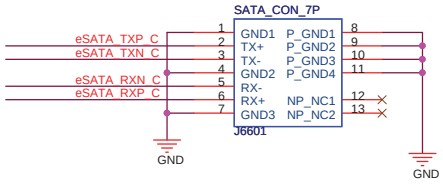
FAN NUT
H5306 CT256B315ID146 GND

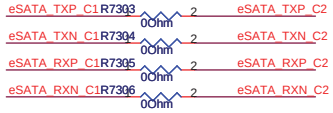
MINI PCI-E CON

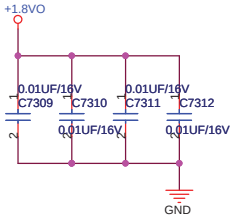


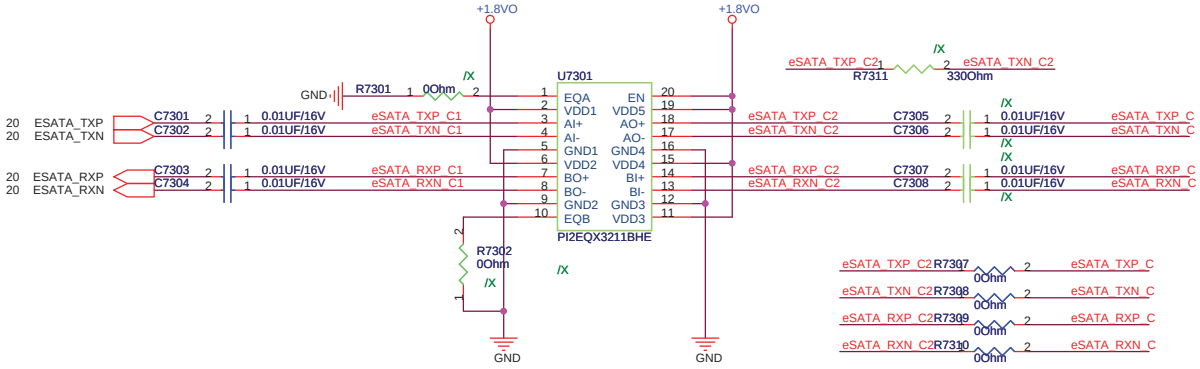
| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title MDC NUT & Hinksink NUT | |
| | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | Sheet 65 of 79 | |

12G15110007M



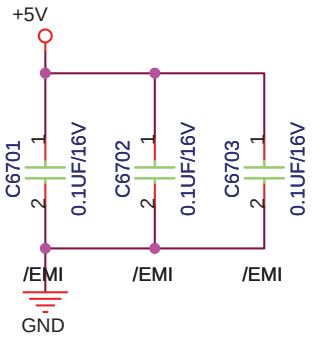



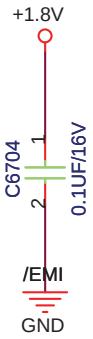



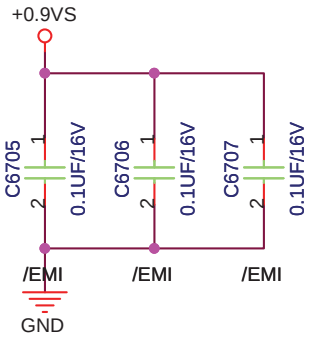



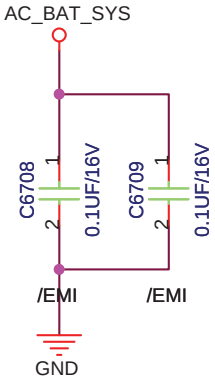


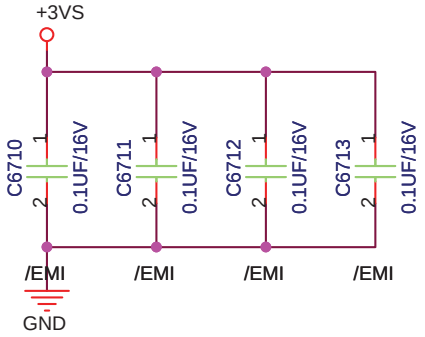

| | | |
|---|---|---|
| Title : E-SATA | | |
| ASUSTeK COMPUTER INC. NB1 | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Friday, August 01, 2008 | Sheet 66 of 79 | |

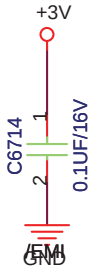


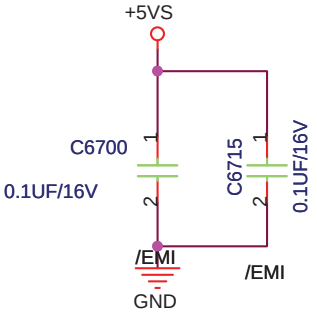



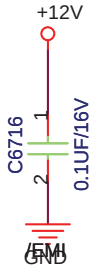




| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : Engineer: <OrgAddr1> | |
| Size: A | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Friday, August 01, 2008 | Sheet 67 of 79 | |

| | | | |
|---|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | | Title : XDP | |
| | | Engineer: <OrgAddr1> | |
| Size: Custom | Project Name: N50A/N51A | | Rev: 1.0 |
| Date: Wednesday, August 06, 2008 | | Sheet 68 of 79 | |

# N50Vm Revision History

| Rev | Date | Description |
|---|---|---|
| 1.0 | 2007-07-28 | Add R4835、C4835 、R2323 |
| | | |
| | | |
| | | |
| | 2007/11/22 | |

| Rev | Date | Description |
|---|---|---|
| | | |



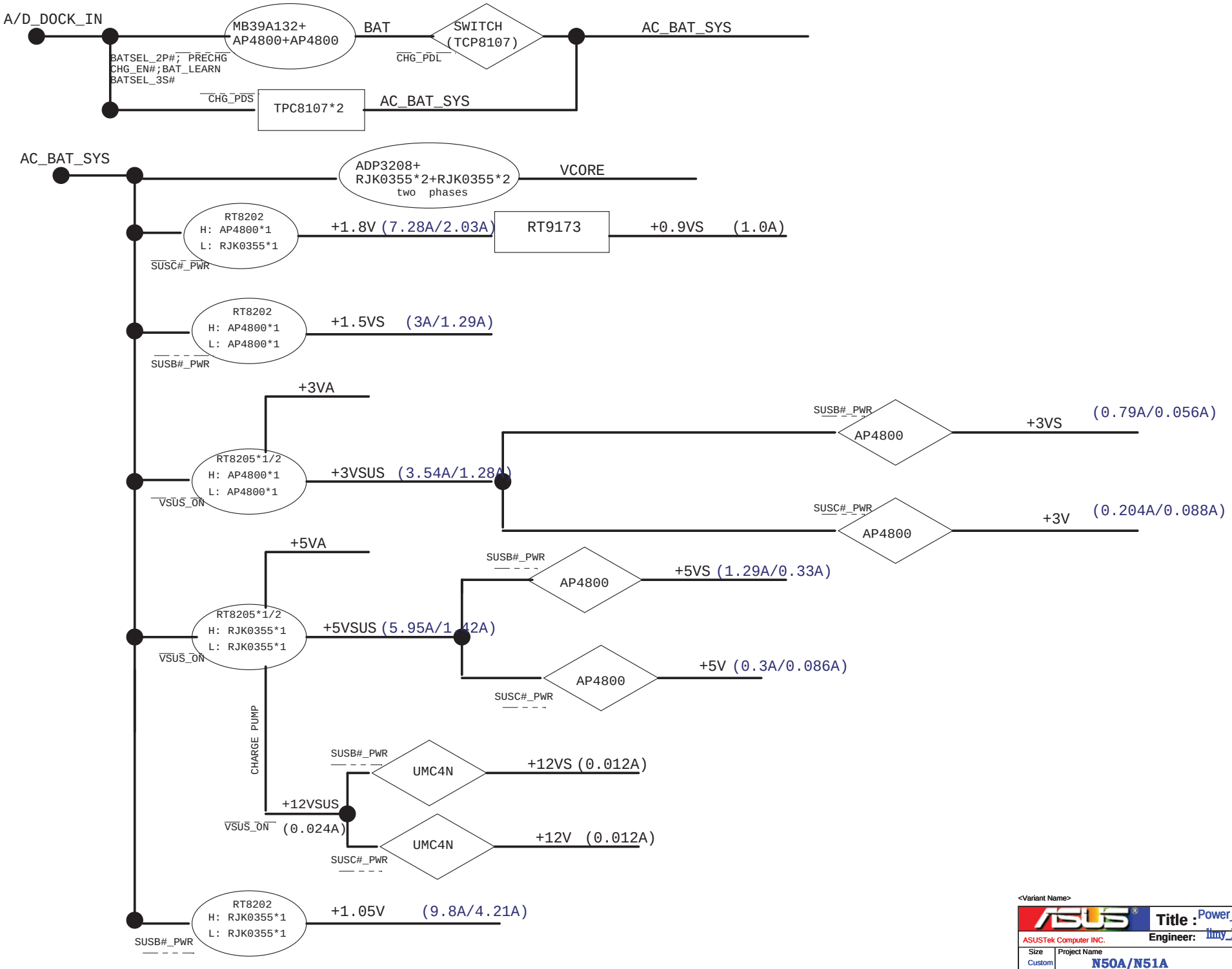
ASUSTeK COMPUTER INC. NB1

Title : HISTORY

Engineer: <OrgAddr1>

| Size | Project Name | Rev |
|---|---|---|
| Custom | N50A/N51A | 1.0 |

Date: Monday, July 28, 2008 Sheet 69 of 79




<Variant Name>

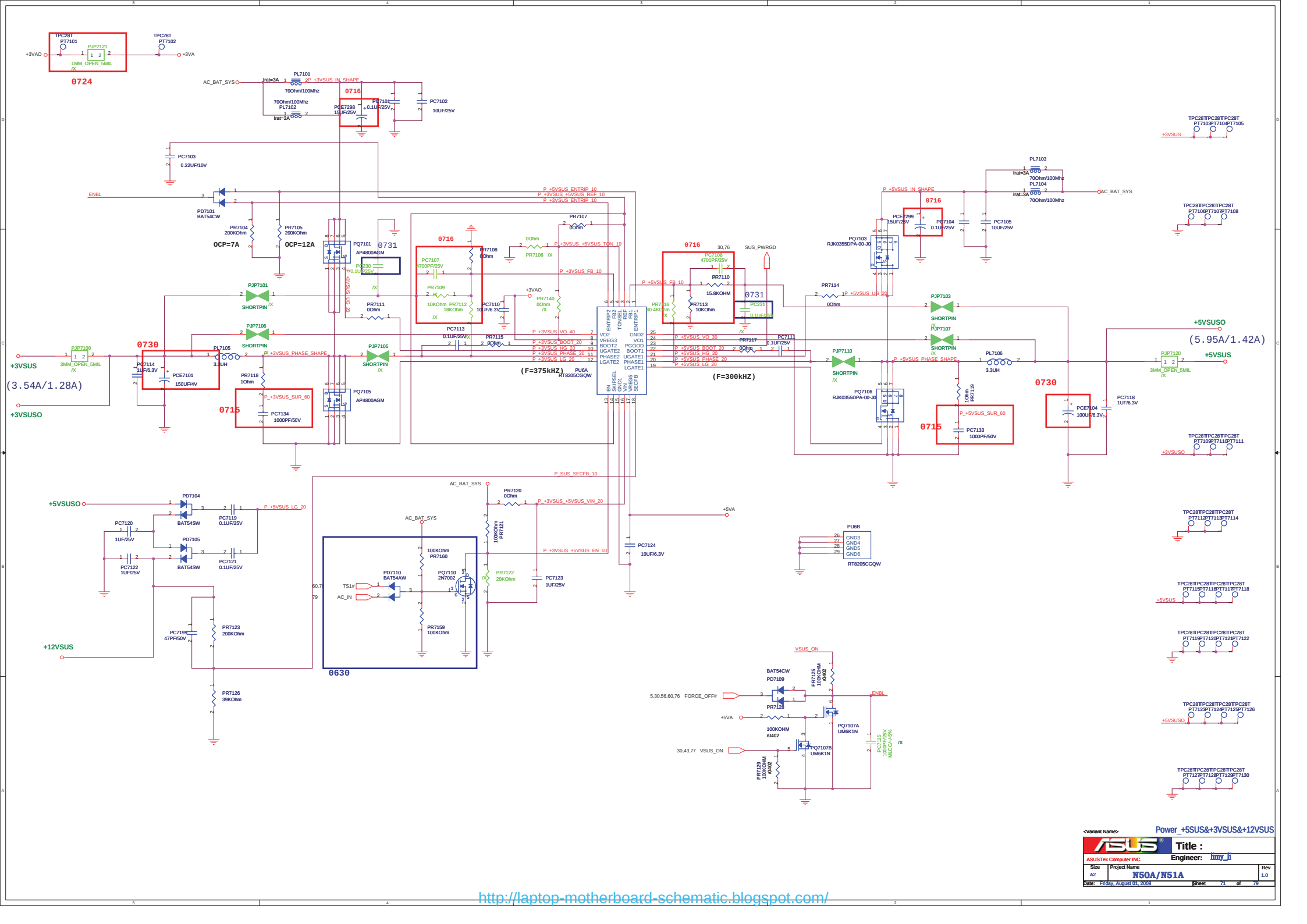
ASUSTek Computer INC.

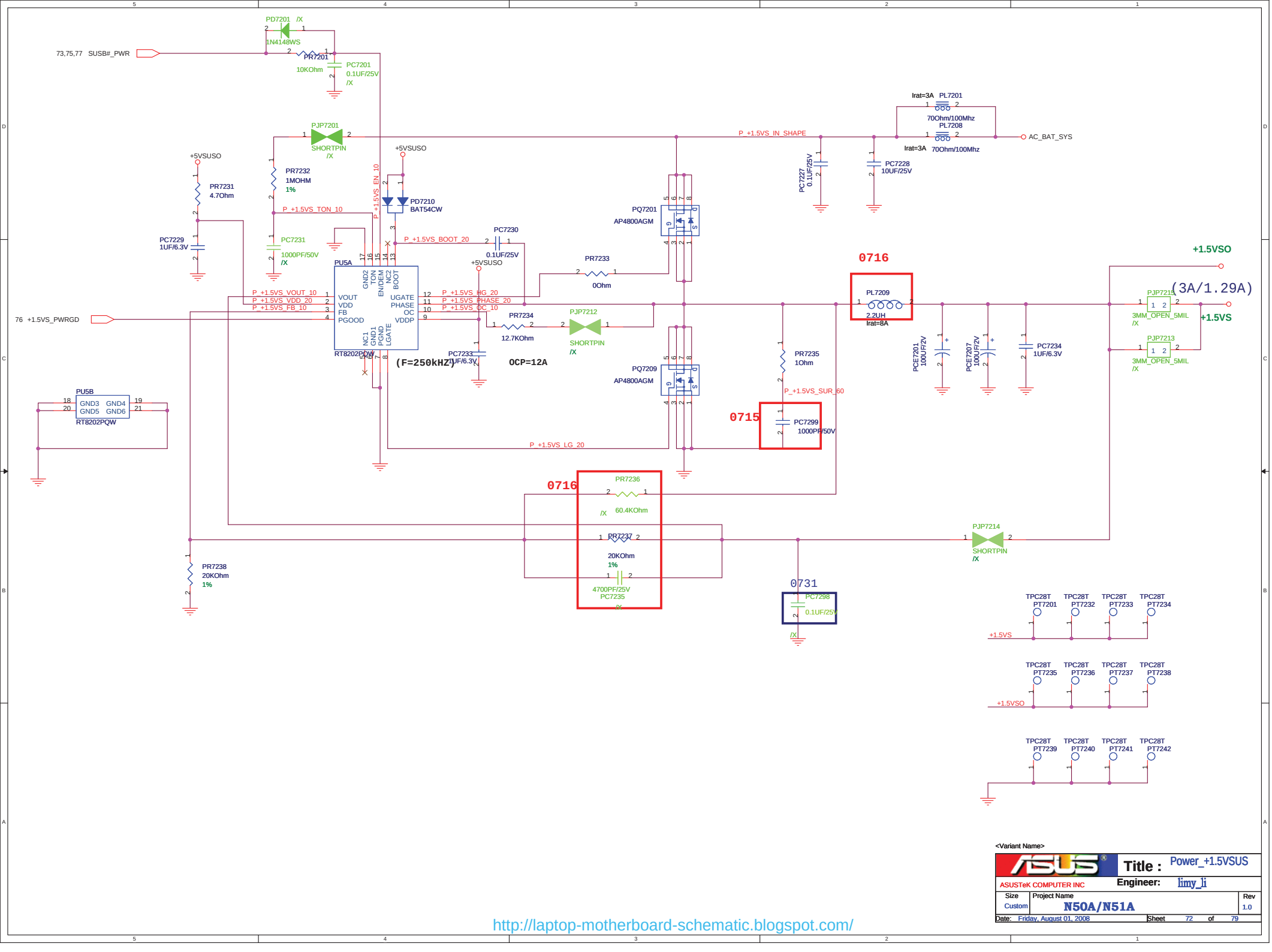
Title : Power_Flow

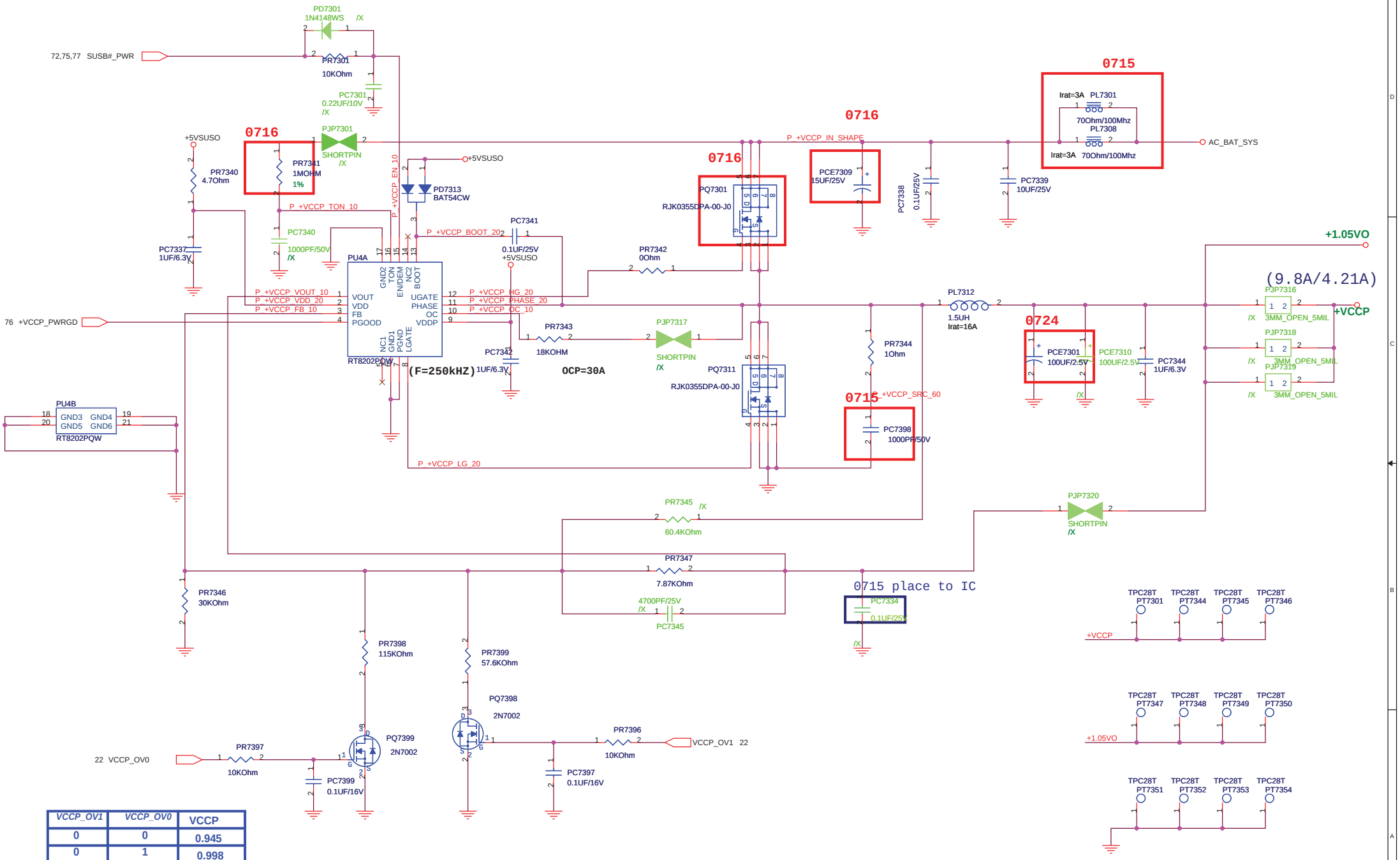
Engineer: Jimy_Ji

| Size | Project Name | Rev |
|---|---|---|
| Custom | N50A/N51A | 1.0 |

Date: Friday, August 01, 2008 Sheet 70 of 79


+3VSUS
(3.54A/1.28A)
+3VSUSO
+5VSUSO
(5.95A/1.42A)
+5VSUS
+12VSUS
(F=375kHz)
(F=300kHz)
PU6A RT8205CGQW
PU6B RT8205CGQW
0724
0730
0731
0716
0715
0630
ENBL
VSUS_ON
FORCE_OFF#
AC_BAT_SYS
SUS_PWRGD
OCP=7A
OCP=12A
http://laptop-motherboard-schematic.blogspot.com/






| VCCP_OV1 | VCCP_OV0 | VCCP |
|---|---|---|
| 0 | 0 | 0.945 |
| 0 | 1 | 0.998 |
| 1 | 0 | 1.049 |
| 1 | 1 | 1.1005 |



<Variant Name>

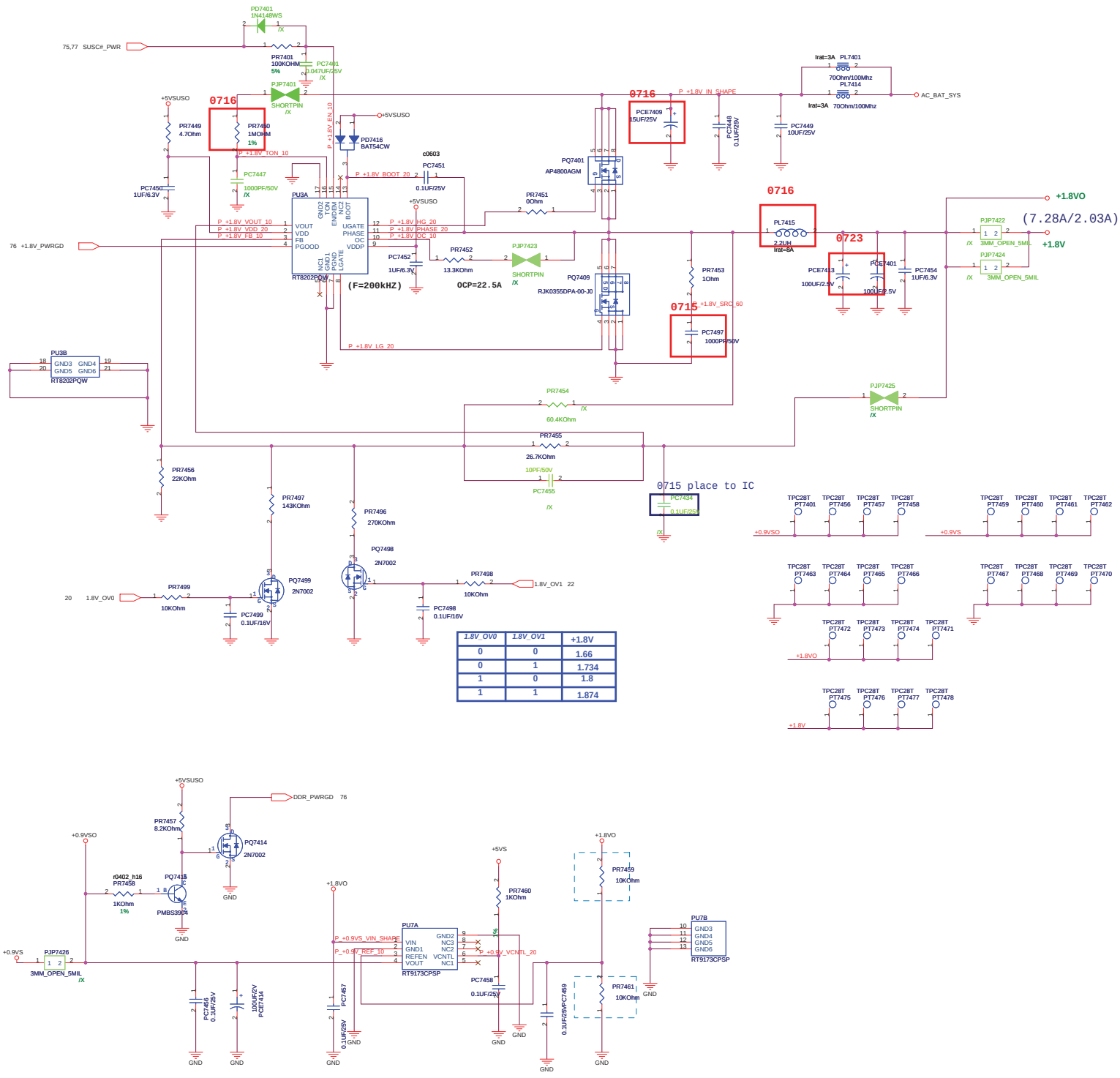
ASUSTeK COMPUTER INC

Title : Power_+VCCP

Engineer: limy_li

| Size | Project Name | Rev |
|---|---|---|
| A3 | N50A/N51A | 1.0 |

Date: Friday, August 01, 2008 Sheet 73 of 79






<Variant Name>

ASUSTeK COMPUTER INC

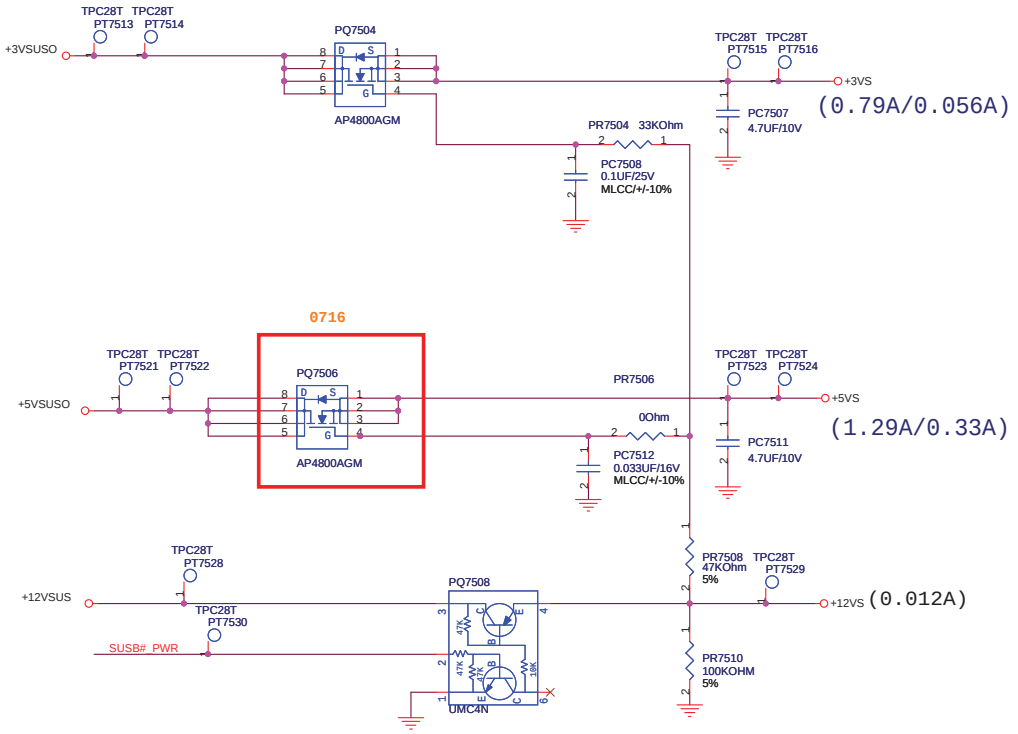
Title : Power_+1.8V&0.9V

Engineer: Jimy_Ji

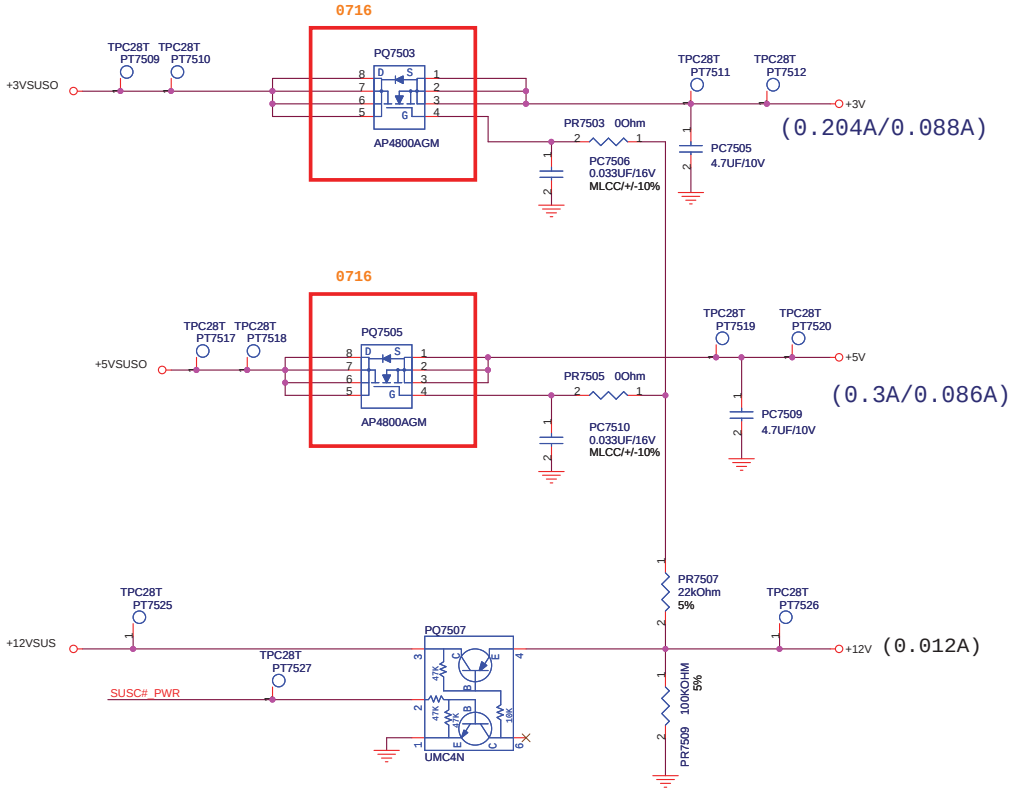
| Size | Project Name | Rev |
|---|---|---|
| A2 | N50A/N51A | 1.0 |

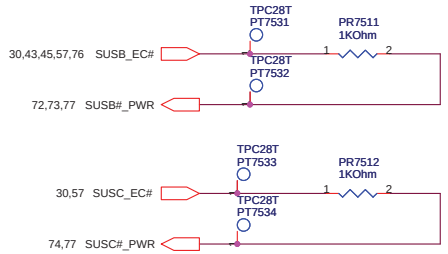
Date: Friday, August 01, 2008 Sheet 74 of 79

## SUSB#_PWR POWER




## SUSC#_PWR POWER

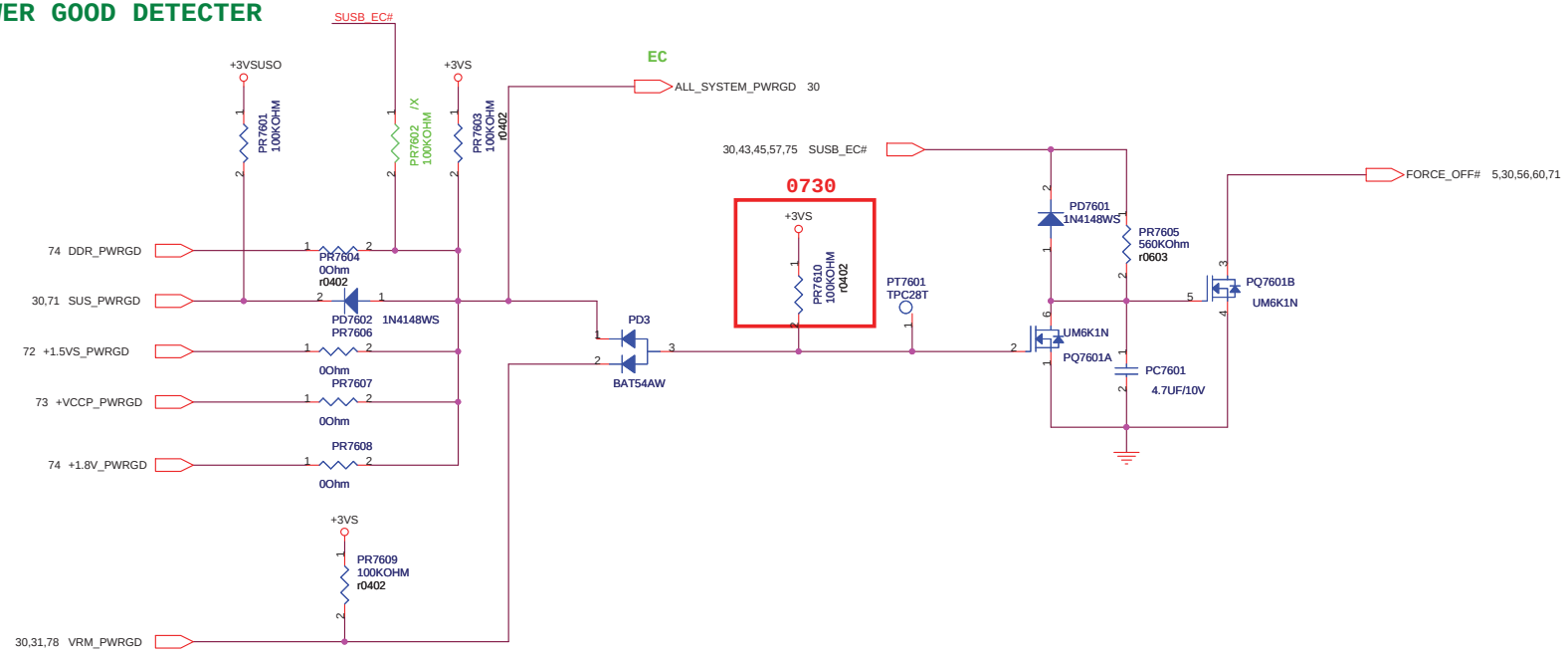



<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : Power_Load_Switch | |
| | Engineer: limy_li | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Tuesday, August 05, 2008 | Sheet 75 of 79 | |

# POWER GOOD DETECTER




<Variant Name>

ASUSTeK COMPUTER INC

Title: Power_good_detecter

Engineer: limy_li

| Size | Project Name | Rev |
|---|---|---|
| Custom | N50A/N51A | 1.0 |

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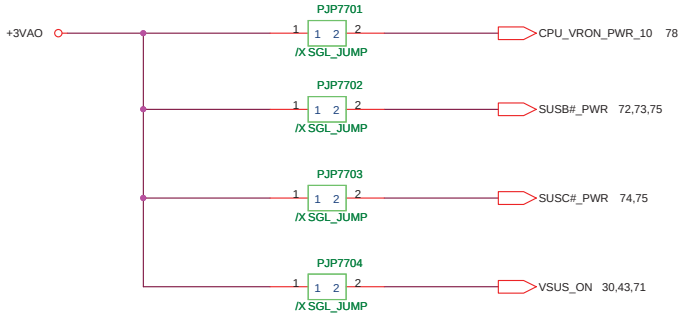
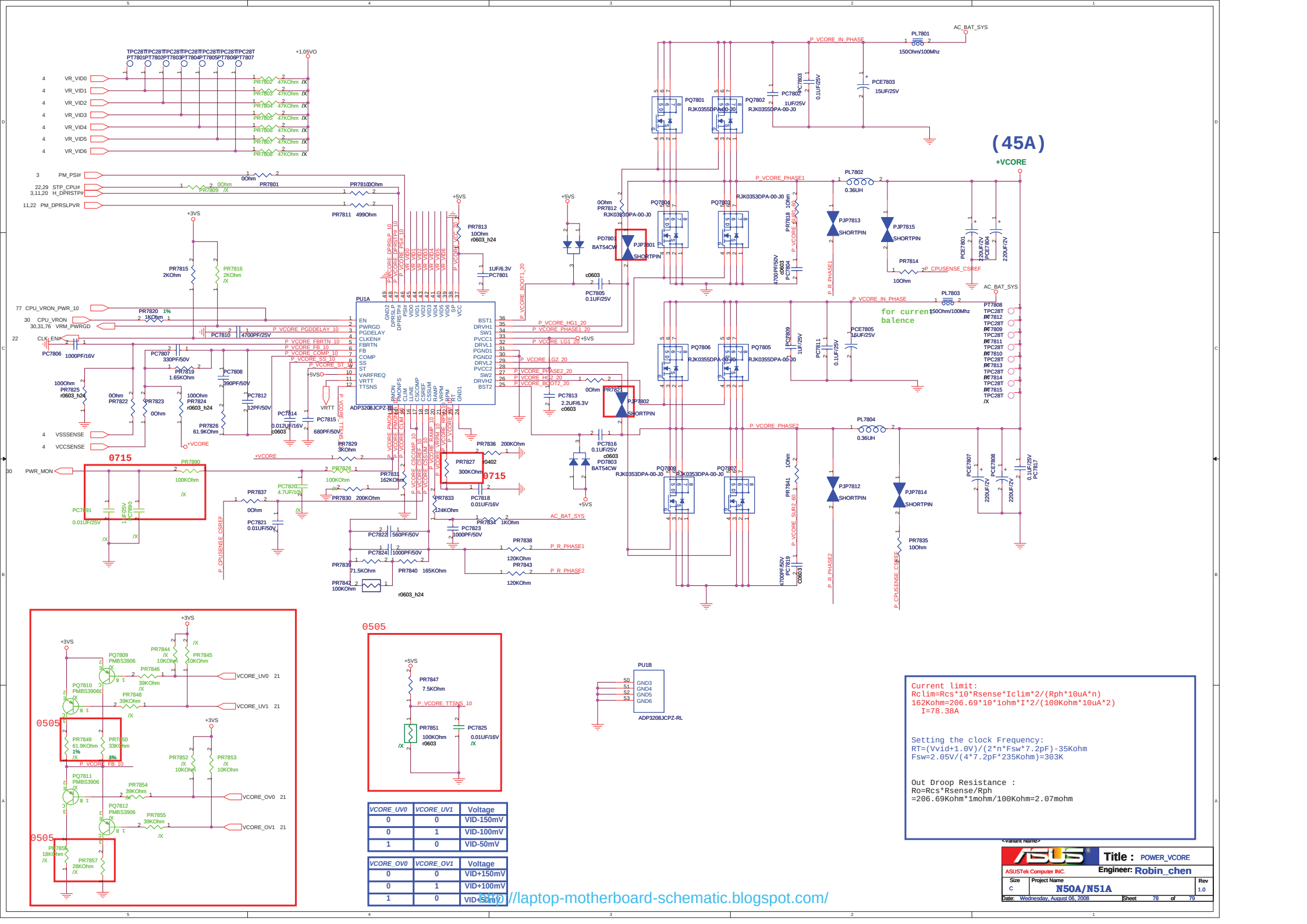



<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : Power_for_test | |
| | Engineer: Robin_chen | |
| Size: Custom | Project Name: N50A/N51A | Rev: 1.0 |
| Date: Friday, August 01, 2008 | Sheet 77 of 79 | |


(45A)
+VCORE
AC_BAT_SYS
PU1A
ADP3208JCPZ-RL
PU1B
ADP3208JCPZ-RL
for current balence
0715
0505
Current limit:
Rclim=Rcs*10*Rsense*Iclim*2/(Rph*10uA*n)
162Kohm=206.69*10*1ohm*I*2/(100Kohm*10uA*2)
I=78.38A
Setting the clock Frequency:
RT=(Vvid+1.0V)/(2*n*Fsw*7.2pF)-35Kohm
Fsw=2.05V/(4*7.2pF*235Kohm)=303K
Out Droop Resistance :
Ro=Rcs*Rsense/Rph
=206.69Kohm*1mohm/100Kohm=2.07mohm
VCORE_UV0 VCORE_UV1 Voltage
0 0 VID-150mV
0 1 VID-100mV
1 0 VID-50mV
VCORE_OV0 VCORE_OV1 Voltage
0 0 VID+150mV
0 1 VID+100mV
1 0 VID+50mV
Title : POWER_VCORE
ASUSTek Computer INC.
Engineer: Robin_chen
Size C
Project Name N50A/N51A
Rev 1.0
Date: Wednesday, August 06, 2008
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http://laptop-motherboard-schematic.blogspot.com/